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Modeling of Integrated Inductors for RF Circuit Design

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Abstract

Integrated Inductors are a fundamental element in voltage-controlled oscillators, low noise amplifiers and LC filters. In this work a model based in lumped elements is presented for the characterization of integrated inductors. With this model, it is possible to design integrated inductors with different topologies, for a wide range of frequencies, by granting the evaluation of important design parameters such as inductance, quality factor and self-resonance frequency. The model used is based on analytical equations and this equations will be explained in detail. In order to validate the model, some comparisons are made against electromagnetic simulations in two different technologies, a 0.13 μm and 0.35 μm CMOS technology. Also, a statistic analysis is presented in order to validate the model over a wide range of geometric variables and the validation is done against electromagnetic simulations for a 0.35-μm CMOS technology. Variable width integrated inductors are also studied as a way of increasing the quality factor of inductors.

In the end, the model is integrated into two different optimizations processes. A single-objective optimization provides the means for an RF designer to design inductors for a given application. On the other hand, multi-objective optimizations provide the means to obtain a trade-off performance curve with a set of the inductors that represent the best inductors for a given technology. Regarding the multi-objective optimization, a novel approach to design integrated inductors is presented. The design methodology uses the multi-objective optimization algorithm integrated with the model as a performance evaluator to analyse the trade-off performances and after the optimization, the front-end obtained is simulated electromagnetically as a fine tuning operation. This method allows accurate results while saving time due to the usage of the lumped element model in a first design stage.

Keywords: Integrated inductors, Variable Width, ASITIC, Optimization

Resumo

Bobines integradas são um bloco fundamental para circuitos como osciladores controlados por tensão, amplificadores de baixo ruído e filtros LC. Nestre trabalho um modelo baseado em elementos distribuídos é apresentado para a caracterização de bobines integradas. Com este modelo é possível projectar bobines integradas de diferentes topologias, e para um diverso espectro de frequências, através da caracterização de parametros muito importantes, tais como, indutância, factor de qualidade e frequência de auto ressonância. O modelo usado é baseado em expressões analíticas e estas vão ser explicadas em detalhe. Para validar o modelo, algumas comparações foram feitas com simulações electromagnéticas com duas tecnologias diferentes, 0.13 μm e 0.35 μm tecnologia CMOS. Um estudo estatístico foi também efectuado para validar o modelo para diferentes variáveis geométricas. Esta validação é feita por comparação com simulação electromagnética para a tecnologia de 0.35-μm. Bobines de espessura variável também foram estudadas como forma de atinigr factores de qualidade mais elevados.

No final, o modelo foi integrado em dois processos de optimização diferentes. Uma optimização mono-objectivo providencia uma forma para o desenhador obter bobines com para uma determinada aplicação. Por outro lado, uma optimização multi-objectivo proporciona uma forma de obter uma curva com os *trade-offs* para cada tecnologia. Esta curva representa as melhores bobines para a tecnologia dada. Para esta optimização multi-objectivo uma nova ideia para desenhar bobines é apresentada. A metodologia de desenho usa a optimização multi-objectivo integrada com o modelo para analisar as *trade-offs* da tecnologia e depois da optimização, a frente obtida é simulada electromagnéticamente para efectuar um acerto e remover o erro ligado ao modelo. Esta metodologia permite poupar tempo devido à integração do modelo numa primeira fase de desenho.

Palavras-chave: Bobines integradas, espessura variável, ASITIC, optimização

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Abbreviations

VCO	**V**oltage **C**ontrolled **O**scillator
LNA	**L**ow **N**oise **A**mplifier
RF	**R**adio **F**requency
CMOS	**C**omplementary **M**etal-**O**xide-**S**emiconductor
DC	**D**irect **C**urrent
IC	**I**ntegrated **C**ircuit
SoC	**S**ystem **o**n **C**hip
EM	**E**lectromagnetic
SRF	**S**elf-**R**essonance **F**requency
MMIC	**M**onolithic **M**icrowave **I**ntegrated **C**ircuit
GaAs	**G**allium **A**rsenide
PGS	**P**atterned **G**round **S**hield
SGS	**S**olid **G**round **S**hield
PDMA	**P**lastic **D**eformation **M**agnetic **A**ssembly
SBDE	**S**election **B**ased **D**ifferential **E**volution
MOEA	**M**ulti-**O**bjective **E**volutionary **A**lgorithms
NSGA-II	**N**on-**D**ominated **S**orting **G**enetic **A**lgorithm-II

1

Introduction

The beauty of wireless connections through radio frequency (RF), for both voice communications and data transmission, has been motivating research work in this field ever since Guglielmo Marconi sent the first radio signal across the Atlantic ocean in 1901 [14]. At the time the motivation was the ability to communicate with people at hundreds of kilometres away. Nowadays, the ability to communicate with people is taken for granted, and the main goal is now to increase the amount of information sent. To accomplish this goal, an increasing demand for bandwidth has pushed new standards in the wireless domain. These new standards evolved towards higher operating frequencies. Besides the importance of the increase of the bandwidth, wireless transmission allows the elimination of a physical connection between receiver and transmitter, which is a key advantage in modern communication systems.

1.1 Background and Motivation

With the explosive growth of the wireless communication market, the demand for fully integrated single chip RF transceiver systems also increased. The most serious candidate for this market seems to be the silicon-based radio frequency integrated circuits technology which offers the most in terms of reliability, low cost and higher integration level. The demand for low-cost radio frequency integrated circuits increased during the last years and a tremendous interest has been generated in on-chip passive components such as resistors, capacitors and inductors. During the past few years design efforts were made with the goal of integrating passive components. Compared to resistors and capacitors which nowadays have several integrated options, with most implementations being easy to model and implement, considerable effort has gone into the design and modelling of

on-chip inductors, which nowadays are a key component in radio frequency, where they are used in tuning, filtering and impedance matching applications.

There are only a few options when integrating inductors, such as on-chip inductors are bond wires and planar spiral geometries. For simulating the inductor performances, there are mainly two options when designing inductors, electromagnetic (EM) simulations or analytical models, either physical or surrogate. While, EM simulations are accurate but time consuming, the already developed models are not sufficiently accurate. The objective of this thesis is to develop a model which is suitable to design spiral integrated inductors of any shape (such as square, hexagonal or octagonal). This model is to be integrated into optimization processes.

1.2 Thesis Outline

The outline of this thesis is as follows. Chapter 2 introduces the basic principles of integrated inductors, such as its physical parameters. Some important effects such as the self-resonance frequency will be introduced and the losses associated with integrated inductors will be briefly explained. A revision of the most important lumped-element models reported in the literature for integrated inductors will also be presented. Advanced structures for integrated inductors will be presented, that reduce the losses associated to the simplest integration techniques.

Chapter 3 the model developed in this thesis is presented. The chapter starts by introducing the segmented model, which is the main feature of the model used. Then the chapter introduces the analytical expressions of the model to calculate resistances and capacitors and how to evaluate the inductance of any type of integrated inductor topology.

Chapter 4 validates the model for two different technologies against field solvers, ASITIC and electromagnetic simulations. Firstly the inductance model is validated in a 0.13 μm CMOS technology against ASITIC and afterwards the model is validated for three different layouts, square, hexagonal and octagonal, with all the inductors having equal turn widths. The model is also validated in a 0.35 μm CMOS technology for an equal turn width octagonal layout. In this case a statistical study was performed with 1000 inductors generated with the latin hypercube sampling technique. The capabillity of the model was also tested for inductors with variable turn widths, commonly denominated tapered width inductors. Again, the inductance model is validated against ASITIC for square layouts. Afterwards an extensive study is made for octagonal tapered width inductors, in order to understand how does the inductors quality factor improve with the tapered width technique.

In chapter 5, the model is integrated into two different optimization processes, one including a single-objective algorithm and a second one including a multi-objective algorithm. The objective of the single-objective optimization is to obtain inductors for a given value of inductance and then compare them with EM simulation. The objective of the multi-objective optimization is to obtain the performance trade-offs which can give

information about the entire design space for a given technology. All the optimizations are done with a 0.35 μm CMOS technology. Conclusions to this work are drawn out in chapter 6 together with future work.

1.3 Thesis Contributions

The work developed in this thesis provided the means to improve the existing literature about the modeling of integrated inductor. This thesis originated six different publications into several different well known international conferences and journals.

1. The first publication, *Analythical Characterization of Variable Width Integrated Spiral Inductors*, on the 20th IEEE MIXDES Conference, introduces the model and explains how to accurately calculate the inductance parameter of several inductor topologies. This paper was given the *Outstanding Paper Award* on that conference.

2. The second publication, A Wideband Lumped-Element Model for Arbitrarily Shaped Integrated Inductors on the 21st IEEE ECCTD Conference, introduced the complete model and its validation is made against EM simulations for a 0.13 μm CMOS technology.

3. The third publication on the 28th DCIS conference is entitled, *A Wideband Lumped-Element Model for Integrated Spiral Inductors*, and shows the ability of the model to design tapered inductors.

4. The fourth publication, on the IEEE COMCAS 2013, shows a statistical study over an high number of inductors, providing therefore a better understanding over the range of geometrical parameters where the model shows accurate results.

5. The fifth publication, on the DoCEIS 2014, shows results for the single-optimization processes.

6. Another publication was made in the International Journal Of Electronics And Telecommunications, as an invitation to extend the paper on the 20th IEEE MIXDES.

It is clear to understand by these contributions that this work developed the topic of integrated inductor modeling and contributed significantly for the existing literature and obtained a strong impact on the RF community.

2

Planar Spiral Integrated Inductors

In this second chapter the basic theory about integrated inductors design will be presented. Afterwards some insights about integrated inductors modelling techniques, such as electromagnetic simulations or lumped element circuits used to characterize inductors will be presented. Special emphasis is given to the well know π-mode and the 2π-model. Finally, advanced structures developed in order to minimize effects that negatively affect the performances of the inductor, such as the series resistance or the capacitances between the metal and the substrate, will be described.

2.1 Integrated Spiral Inductor Basic Insights

2.1.1 Integrated Inductor Geometries and Basic Topologies

Integrated inductors are usually fabricated using the outer metal layers of the standard CMOS processes. This is done to avoid coupling effects with the substrate. Some processes offer the possibility to use a thicker metal layer that allows a reduction of the resistivity of the metal. The basic structure of an integrated inductor is made up of one or more metal tracks in parallel forming one or several concentric turns, requiring a minimum of two metal layers and one via connection between them for inductors with 2 or more turns. In order to design an inductor it is important to consider both the vertical and lateral geometries of the layout. In Fig. 2.1 it is possible to observe a three dimensional square spiral inductor.

Square spirals are popular due to its easy layout. However, some other layouts can be used to improve the inductor performance. Layouts such as hexagonal and octagonal have already been reported. If desired, a circular layout may be approximated using a

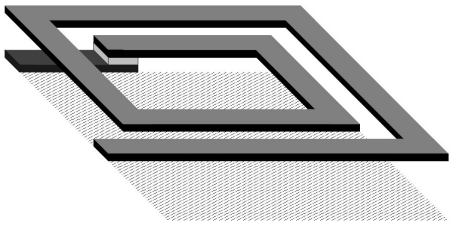


Figure 2.1: 3-D view of a square spiral inductor [1].

polygonal with many sides. Fig. 2.2, Fig. 2.3, Fig 2.4 and Fig. 2.5 show the different layouts, for square, hexagonal, octagonal and circular respectively.

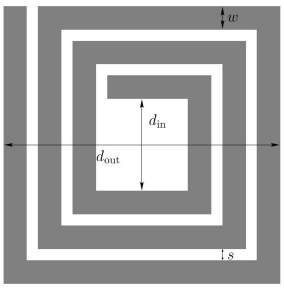


Figure 2.2: Square spiral inductor [1].

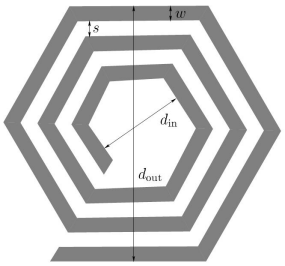


Figure 2.3: Hexagonal spiral inductor [1].

The geometry of a planar spiral inductor is defined by five geometric parameters:

1. number of turns, n,
2. metal width, w,
3. spacing between turns, s,
4. any of the following: the outer diameter D_{out} or the inner diameter D_{in},
5. number of sides, N.

The most important performance characteristics for spiral integrated inductors are the inductance (L), the quality factor (Q) and the self-resonance frequency (SRF). The five geometric parameters presented are responsible for the definition of inductance. However,

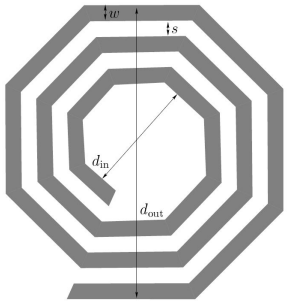


Figure 2.4: Octagonal spiral inductor [1].

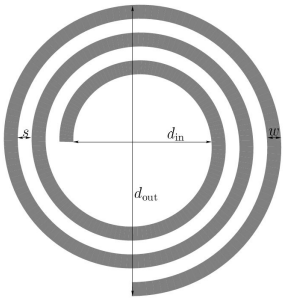


Figure 2.5: Circular spiral inductor [1].

lateral and vertical dimensions are used to define the other two important performance parameters, Q and SRF, as it will be explained afterwards. In Fig. 2.6, a typical cross section of an inductor is presented.

Integrated planar inductors can be defined by a simple model at low frequencies (neglecting parasitic capacitances) as shown in the Fig. 2.7.

For these conditions, the input equivalent impedance can be written as follows:

$$Z_{eq} = R_s + j\omega L_s \tag{2.1}$$

where R_s and L_s are the series resistance due to the conductivity of metal and the inductance of the component, respectively. A physical interpretation of both parameters will be discussed later.

2.1.2 Inductance

Inductance, L_s, is the relationship between the total current flow through the spirals and the magnetic field generated by this current. The relationship between the self-inductance L of an electrical circuit in Henry, given by,

$$v = L \cdot \frac{di}{dt} \tag{2.2}$$

where v denotes the voltage in Volt and i the current in Ampere. As we may conclude, the voltage across an inductor is equal to the product of its inductance and the time rate of

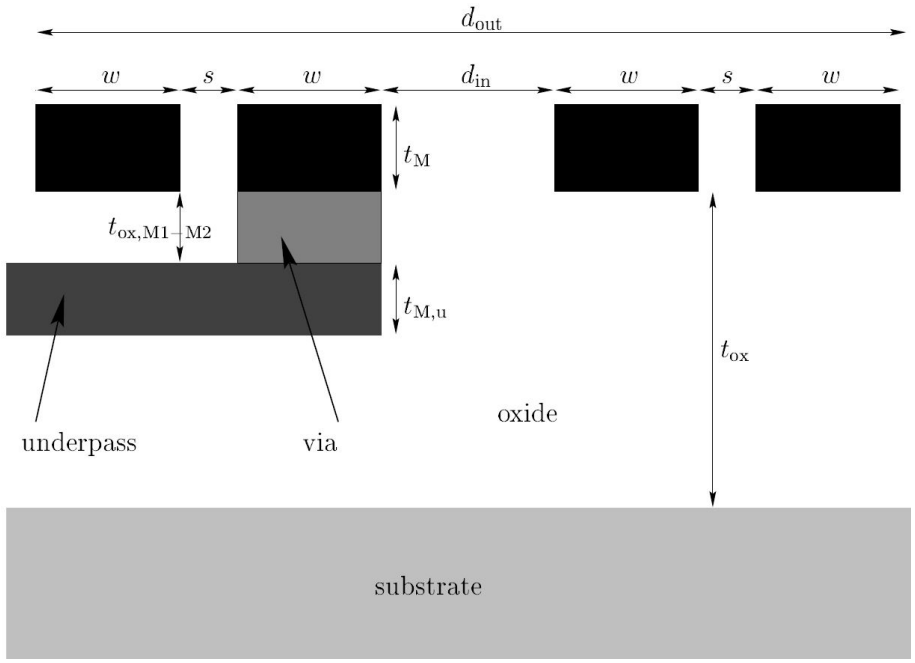


Figure 2.6: Vertical cross section of a square spiral [1].

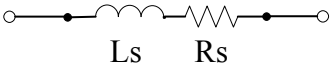


Figure 2.7: Simple model of inductor at low frequency.

change of the current through it. All integrated conductors have some inductance, which may provide either beneficial or detrimental effects. There are three types of inductances, as it can be seen in the following equation,

$$L_s = L_0 + L_{M+} + L_{M-} \tag{2.3}$$

where:

- L_s is the total inductance of the inductor.
- L_0 is the auto inductance associated to each coil.
- L_{M+} is the mutual inductance between the coils where the direction of the current flow generates magnetic fields lines in the positive direction.
- L_{M-} is the mutual inductance between the coils where the direction of the current flow generates magnetic fields lines in the negative direction.

Another method and possibly the more general method to obtain the equivalent inductance of planar inductors is from the equivalent impedance, shown in equation 2.4.

$$L_s = \frac{Im(Z_{eq})}{2\pi \cdot f} \tag{2.4}$$

2.1.3 Quality Factor

The quality factor, Q, is an extremely important figure of merit when designing a integrated inductor. Basically, it describes how good an inductor works as an energy-storage element. In the ideal case, inductance is pure energy-storage element (Q approaches infinity), while in reality, parasitic resistances and capacitances reduce the value of Q. This is caused by the fact that parasitic resistance consumes stored energy, and the parasitic capacitance reduces inductance (the inductor even turns capacitive at high frequencies. Several different definitions of quality factors for inductors have been used in the literature [2]. The most general definition for Q-factor is given by Eq. 2.5,

$$Q = 2\pi \cdot \frac{E_{stored}}{E_{dissipated}} \tag{2.5}$$

where E_{stored} is the energy stored in the passive component, whereas $E_{dissipated}$ is the energy loss in one cycle. A good approximation to understand what the quality factor means in to think that Q-factor is a measure of the ratio of the desired quantity of inductance to the undesired quantity of resistance. Another equation, which is widely used for calculate the inductor quality factor is therefore given by,

$$Q = \frac{Im(Z_{ind})}{Re(Z_{ind})} \tag{2.6}$$

where Z_{ind} is the impedance of the inductor.

2.1.4 Self-Resonance

At low frequencies, the inductance of an integrated inductor will be relatively constant, and this zone is called by some authors the flat-bandwidth region [15]. The inductor should work in this flat-bandwidth zone, where the inductance value has not changed much from DC value and the quality factor is near its peak, but with a positive slope. When the operating frequency increases, the effect of parasitic capacitances start to increase and the inductance value is no longer constant. Finally, at one frequency point, the admittance of the parasitic capacitances will cancel the inductance of the inductor and it stops behaving as an inductance source and will act as a purely resistive load to the circuit. The point in frequency where this phenomenon happens, is called the self-resonance frequency (SRF). At this point the inductance, L, is equal to zero, which also brings the quality factor to zero. This phenomenon can the observed in Fig. 2.8, where a typical integrated inductor characteristics is presented.

Due to this phenomenon it is possible to understand that integrated inductors have limited bandwidth over which they can be used. Since parasitic capacitances increase in proportion to the size of the inductor, the SRF decreases as the size of the inductor increases [14].

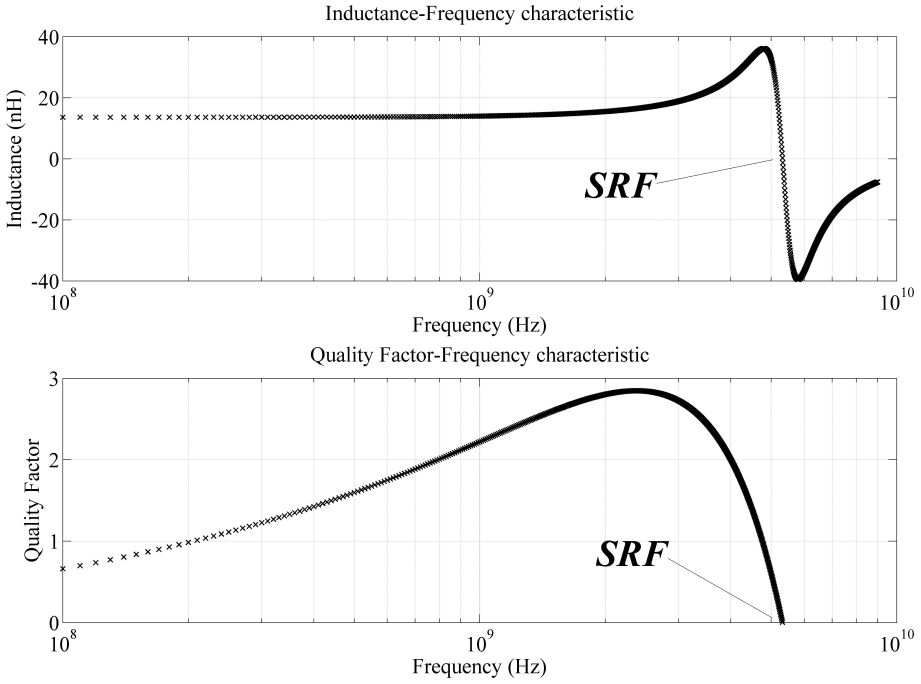


Figure 2.8: Self-Resonance frequency shown both in inductance-frequency graph and quality factor-frequency plots.

2.1.5 Losses in Integrated Inductors

There are several mechanisms and effects that can produce losses in integrated inductors. The most common and most significant losses are conductive losses, which are related with the resistance of the metal lines. Integrated inductors are further affected by the internally induced losses, which are caused by the increase of frequency and temperature. As the frequency and temperature raises, the resistance of the metal lines show a significant growth, which leads to more losses.

The externally induced losses, are another problem that affects integrated inductors in silicon substrates. This losses are created by a time-varying flux which creates a phenomenon called Eddy currents. Integrated inductors also have the so called magnetization losses, which are related to the fact that for magnetic materials, the magnetic permeability μ is non-linear and frequency dependent and dissipative [16].

As previously said, a spiral is usually implemented in the topmost available metal, because of its low resistivity and lower parasitic capacitances to substrate. In sub-micron CMOS technologies, the top metal layer has the largest thickness, thereby minimizing the DC series resistance of the inductor. Due to the large variety of S_i technologies and its different substrate resistivity values (i.e., 0.01–100 Ω-cm) [2], the design of integrated inductors becomes quite complex. The physical parameters of inductors have significant importance into the increase of effects such as the Eddy current and the skin depth effect. For example, for a lower D_{in}, the Eddy current effect increases. These different effects

and losses are discussed in the following sections.

2.1.5.1 Sheet Resistance and Skin Depth

The sheet resistance arises from the resistivity of the metal. At low frequencies, the resistance of the inductor is given by Eq. 2.7,

$$R_{DC} = \frac{l \cdot \rho}{w \cdot t} \tag{2.7}$$

where l is the conductor length, ρ is the resistivity of the material, w is the metal width and t the metal thickness. However, at high frequencies, another effect comes into play. Electromagnetic waves suffer attenuation as they enter a conductor. As the frequency approaches the GHz range, the distance that the waves can penetrate becomes comparable to the size of the metal line. The problem is that the current becomes concentrated around the outside of the conductor, with much less current flowing in the center of the conductor. This effect is shown in Fig. 2.9, where the current concentration is defined by the colour red. This is known as skin effect, and can be explained by the tendency of an alternating electric current (AC) to become distributed within a conductor such that the current density is largest near the surface of the conductor, and starts decreasing into the center. The electric current flows mainly at the "skin" of the conductor, between the outer surface and a level called the skin depth. The skin effect causes the effective resistance of the conductor to increase at higher frequencies where the skin depth is smaller, thus reducing the effective cross-section of the conductor.

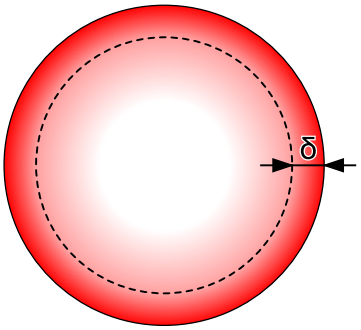


Figure 2.9: Skin depth definition through a circular conductor.

The skin depth, δ, is given by the following equation [17],

$$\delta = \sqrt{\frac{\rho}{\pi f \mu}} \tag{2.8}$$

where f is the frequency and μ is the permeability of the metal. Due to this effect the series resistance of an inductor is commonly stated as follows [17],

$$R_{rf} = \frac{l \cdot \rho}{w \cdot \delta \cdot t_{eff}} \tag{2.9}$$

where t_{eff} is given by Eq. 2.10 [17].

$$t_{eff} = (1 - e^{-t/\delta}) \tag{2.10}$$

The DC sheet resistance of a spiral coil can be reduced by using a thicker metallization. Several thin metal layers can be connected or shunted together to realize a thick metal layer and therefore reduce the sheet resistance. Alternatively, high-conductivity conductors such as copper or gold can be used instead of the aluminium, which is by far the most commonly used in S_i technologies [18]. Advanced S_i technologies (both S_i CMOS and S_iG_e B_iCMOS) have a very thick copper interconnection layer as the last metal. With these technologies inductor Q-factors can easily approach those typically found on semi-insulating substrates [2]

2.1.5.2 Eddy Currents

Eddy currents are electric currents that appear in the inner turns of the integrated inductors created by a changing magnetic field in the conductor. These circulating currents have inductance and thus induce magnetic fields. These fields can cause repulsive, attractive, heating effects among others [2]. Consider a n-turn spiral inductor as shown in Fig. 2.10. The current I_{coil} is the induced current, which has an associated magnetic flux, B_{coil}. The magnetic flux lines enter the page plane at the far end of the turn n and come out of the page plane in the center of the coil, where they have maximum intensity. When there is not enough hollow space in the center of the coil, a large part of the magnetic flux also goes through the inner turns.

According to Faraday-Lenz's law, when a conductor is moved into a magnetic field or a conductor is placed in a time-varying magnetic field, eddy currents are induced in the conductor in the direction where their self-flux is opposite to the applied magnetic field. Thus, as shown in Fig. 2.10, circular eddy currents I_{eddy} are generated due to magnetic fields that go through the inner turns, and an opposing magnetic field, B_{eddy}, due to eddy currents is established. The eddy current loops produced within the trace width cause non-uniform current to flow in the inner coil turns. Because this eddy currents are induced due to time-varying magnetic fields, their values are a strong function of frequency, and it is possible to estimate the critical frequency at which this effects start being significant. The critical frequency f_c at which the current crowding begins to become significant is given by [2],

$$f_c = \frac{3.1 \cdot (w + s)}{2\pi \cdot \mu \cdot w^2} \cdot R_{sh} \tag{2.11}$$

where, μ is the inter-space permeability and R_{sh} is the sheet resistance of the trace.

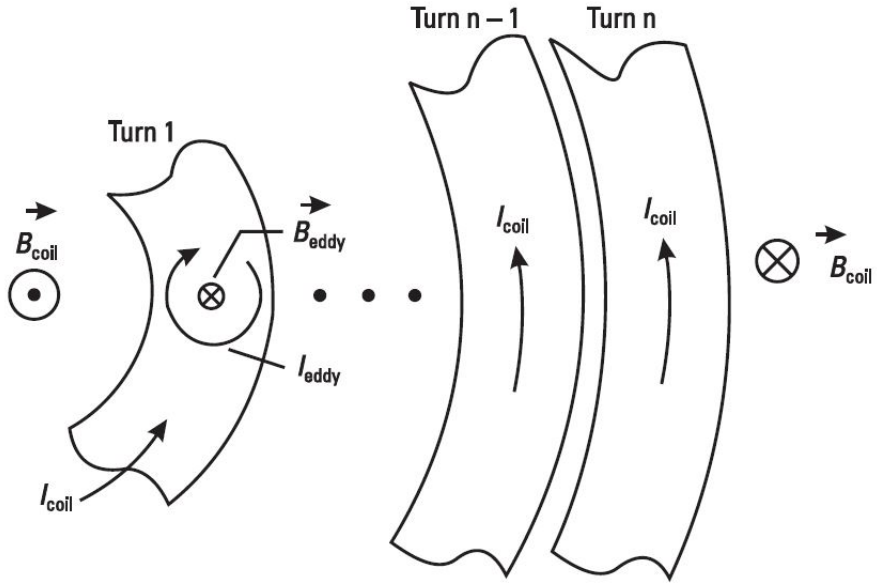


Figure 2.10: Excitation and eddy currents, and fields in a coil. I_{coil} is the excitation current [2].

2.1.5.3 Magnetic Losses

In heavily doped S_i substrates, currents induced by the penetration of the magnetic fields into the substrate cause extra resistive loss. Consider Fig. 2.11, which shows magnetic field flux lines associated with the coil excitation current. The flux lines uniformly surround the inductor and penetrate into the substrate. As discussed above, due to the Faraday-Lenz law, loops of eddy currents flow in the low-resistivity substrate underneath the coil, with higher current density closer to the coil. The direction of I_{sub} is opposite to the direction of I_{coil} , giving rise to extra substrate loss. Because this loss is associated with magnetic fields, it is commonly referred to as magnetic or inductive substrate loss. Substrates with high resistivity have negligible magnetic loss. In summary, by using narrow conductors that meet skin effect requirements ($w \simeq 3d$) in the inner turns, using a hollow coil design, and using compact area coils, one can keep the substrate loss to a minimum. Because the magnetic field in a small coil penetrates less deeply into the substrate, eddy current loss is not as severe as for large coils. Therefore, an optimum solution, in terms of inside dimensions and coil area for a given substrate, can be found.

2.2 Integrated Spiral Inductor Modelling

The determination of integrated inductors behaviour can be made through two different approaches. One of these approaches, is through a field solver or EM Simulator. The other is through lumped circuit models. In the next sections these two approaches are

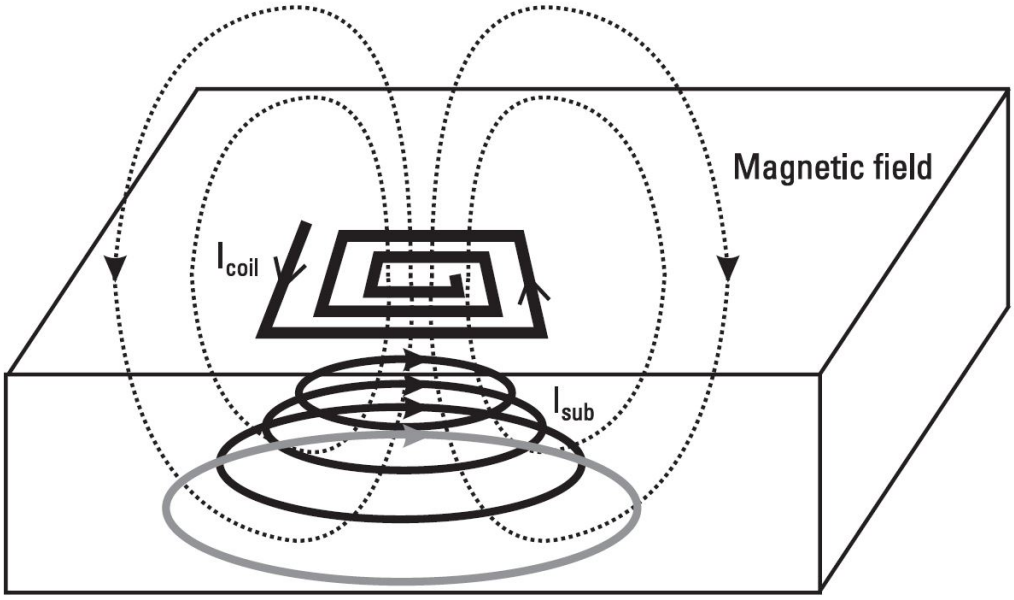


Figure 2.11: Currents and fields in a coil printed on a lossy S_i substrate [2].

discussed.

2.2.1 EM Simulations and Field Solvers

Electromagnetic field solvers, commonly called field solvers, are specialized programs that solve Maxwell's equations directly. There are several 3-D electromagnetic simulators that solve Maxwell's equations numerically, such as ADS Momentum, $Maxwell$, $EM\text{-}Sonnet$ and $MagNet$ [19] [20] [21]. Although accurate, these simulators are computationally intensive, both in memory and time. Thus, while these field solvers are suitable for accurately simulating simple structures, they are not suitable for simulating large three dimensional structures with multiple segments.

Integrated spiral inductors require long simulation times and access to fast processors as well as availability of substantial memory. As it was previously said, these factors are aggravated by commonly encountered situations where the spacing between conductors is small compared to their width [14]. EM simulators require a complete specification of the substrate as well as the definition of all metals and vias of the technology. This means that the designer must have some expertise with electromagnetic solvers and the technology parameters must be available. For the reasons noted above, field solvers are not a practical option for on-chip inductor design. To alleviate some of these issues custom field solvers, geared specifically for the simulation of on-chip spiral inductors and transformers, have been developed. These tools achieve faster simulation speeds by ignoring retardation effects so that magneto-static and electrostatic approximations may be used to quickly solve the field matrices. Some popular spiral inductor and transformer

simulators such as SPIRAL and ASITIC [22] are available. However the use of these tools complicates the interface between the inductor model and the circuit simulator (such as SPICE). The best way to incorporate these field solvers in the design flow is to use them first to generate a library of inductors that span a wide design space and then link that library to the circuit simulator. Unfortunately, this requires new libraries to be generated for every process or, worse, an existing library to be updated even if only a few process parameters are changed [1]. Due to the previous reasons, field solvers are best suited to verify results rather than design and optimize integrated inductor circuits.

2.2.2 Lumped Element Circuit Models

The disadvantages of the 3-D EM simulations indicate the need for a model that can be incorporated into a spice like simulator, in order to reduce the simulation time. Significant work has gone into modelling spiral integrated inductors using lumped element circuits. This section will present state-of-the-art modelling of inductors through lumped element circuit models.

The first lumped element circuit used to model a spiral inductor was a RLC circuit in 1980 [3]. Even though the authors were considering the work to be used in air core inductors for high power, DC-DC conversion circuits, this model, shown in Fig. 2.12, was the starting point for all the following ones.

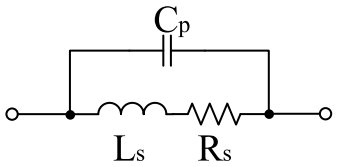


Figure 2.12: First RLC circuit used to model an integrated inductor.

Four years later, a MMIC spiral inductor was modelled with a π circuit in [23], like shown in Fig. 2.13. The name π circuit, adcomes from the fact that the circuit looks like the greek letter π. Normally the L_s and R_s are called the series branch whereas the capacitance to the ground is called the shunt branch.

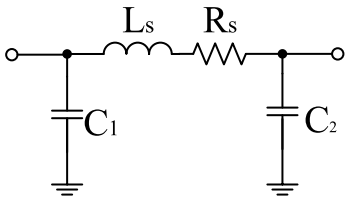


Figure 2.13: First π model used to model an integrated inductor.

In 1985 [24], microstrip spirals were modelled with a π circuit that used a capacitance in parallel with the series branch. This equivalent circuit is shown in Fig. 2.14 [25].

Afterwards the model from [24], was improved to a model that added resistors to the shunt branches of the π circuit to model the leakage currents to ground [26]. This work

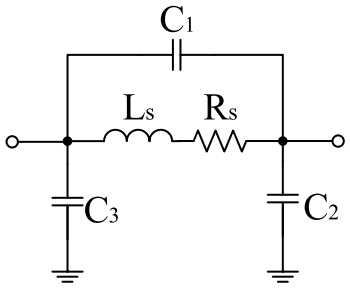


Figure 2.14: First π model that utilized the RLC branch from [3].

was developed in the context of GaAs MMICs [25] ans the circuit is shown in Fig. 2.15

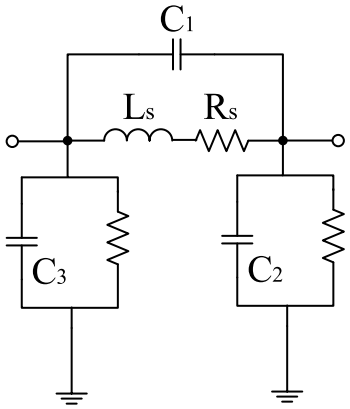


Figure 2.15: First π model with a resistor to model the leakage current.

In 1989, an effort was made to extend the frequency range of the π model by increasing the complexity of the model. This new model blocked the DC leakage current to ground by replacing the shunt branches with a series RC pair [27]. In 1994, the first model was improved to the circuit presented in Fig. 2.16. This would became the most common spiral inductor model for silicon processes. It has the now common RLC triple in its series branch, its shunt branches have a DC blocking capacitor in series with a parallel RC pair [28].

Many authors have attempted to find empirical formulas to extract the component values in the extracted model from the physical properties of the spiral inductor [29] [30]. However this model presents a problem reported in several published works, which is the need to increase the viable bandwidth of usage [25]. In [31], for example, R_s is replaced by a transmission line element. Additionally, completely new and inventive perspectives have been published to increase the accuracy of extracted models. In 1997, a spiral inductor was represented as a long transmission line [32]. An important development was made in [33]. This work presented for the first time a model which had in account the effect of the leakage current that bypasses the spiral inductor by flowing in the substrate, through the introduction of a resistor between the two shunt branches of the π model, as shown in Fig. 2.17. The same work introduced for the first time the double π model, as shown in Fig. 2.18.

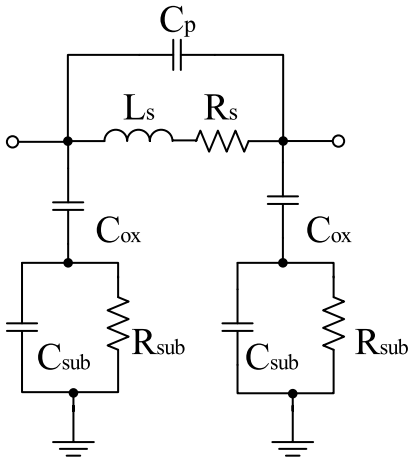


Figure 2.16: Common π model for silicon substrates.

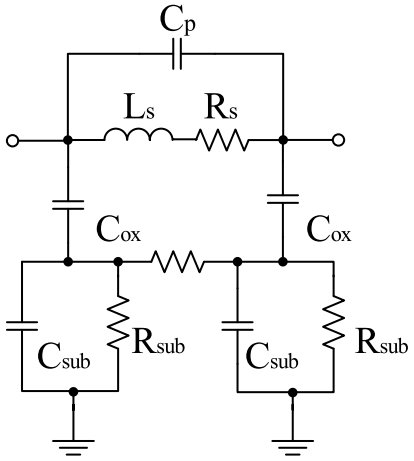


Figure 2.17: π model for silicon substrates with leakage current resistor.

In 1997, Yorgos K. Koutsoyannopoulos, proposed a model which is the starting point for this thesis. The model divided the inductor into segments and then considered the self and mutual inductance of each segment [34] [35]. This model will be explained in detail in section 3.1. In 2002, [36] and [37], introduced the so called skin effect model, as shown in Fig. 2.19. This would become very common and it is a variant of the simple π model, in addition it had a parallel RL branch in series with the L_s and R_s.

In [38], additionally physical effects were considered, such as the proximity effects, which are those effects due to change in current distribution within a conductor caused by nearby conductors. A big improvement into the integrated inductor modelling came in May 2002 with the introduction of inductive coupling between inductors in the extracted models. The topology presented in [39] is based on the π model. The main inductance in the series branch is coupled to one or more unconnected RL loops. These additions are meant to model eddy currents in the substrate. This type of inductive coupling has continued to be popular. Another attempt to include the eddy currents into a model was presented in [40]. In this proposed model, the π model is modified with the

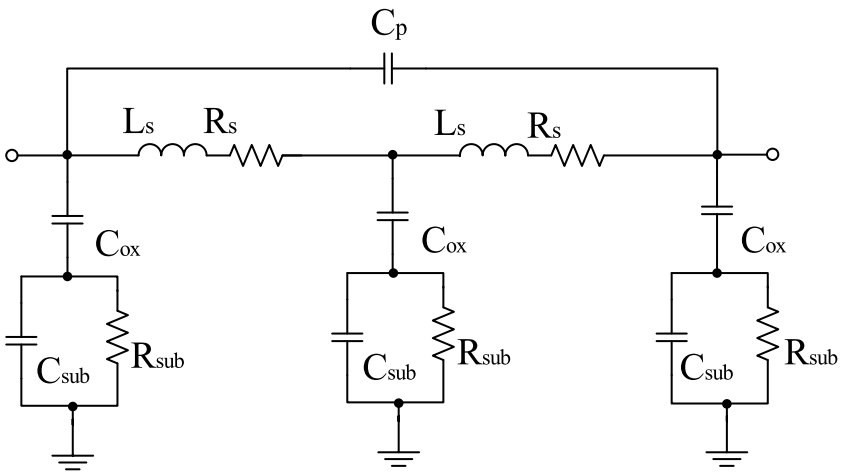


Figure 2.18: Double π model for silicon substrates.

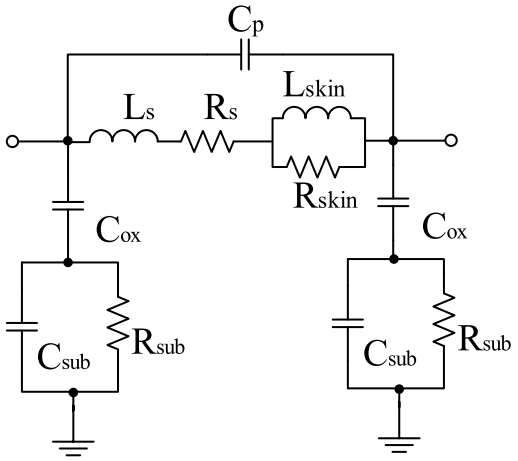


Figure 2.19: π model for silicon substrates considering the skin effect.

series RL connected in parallel with the resistor in the series branch.

In Fig. 2.20, a complex model is presented. This model was proposed in [41]. This model would also go on to become rather popular [25]. It is meant to include skin-effect, proximity effects and the substrate conductivity in a twenty-two element topology with two mutual inductances. Some authors also proposed simpler methods for extracting the component values, for example, Kim, Han and Liu present the extraction of the components through the admittance parameters [42]. In [43] two and three port, double π, skin-effect models are presented and in [44] some additional elements were added to the simple π model, but they are considered "without any physical meaning". A new approach came in 2003, when [45] outlined the use of a modified T instead of a π model. The author also approached the problem from a new perspective by starting with a modified T model normally used to model transmission lines. This transmission line equivalent Modified T model is then developed into one that proves to be a suitable wideband model for spiral inductors for LTCC, this model is shown in Fig. 2.21.

[46] demonstrated the use of a ladder of Simple Models. Using the last reference as

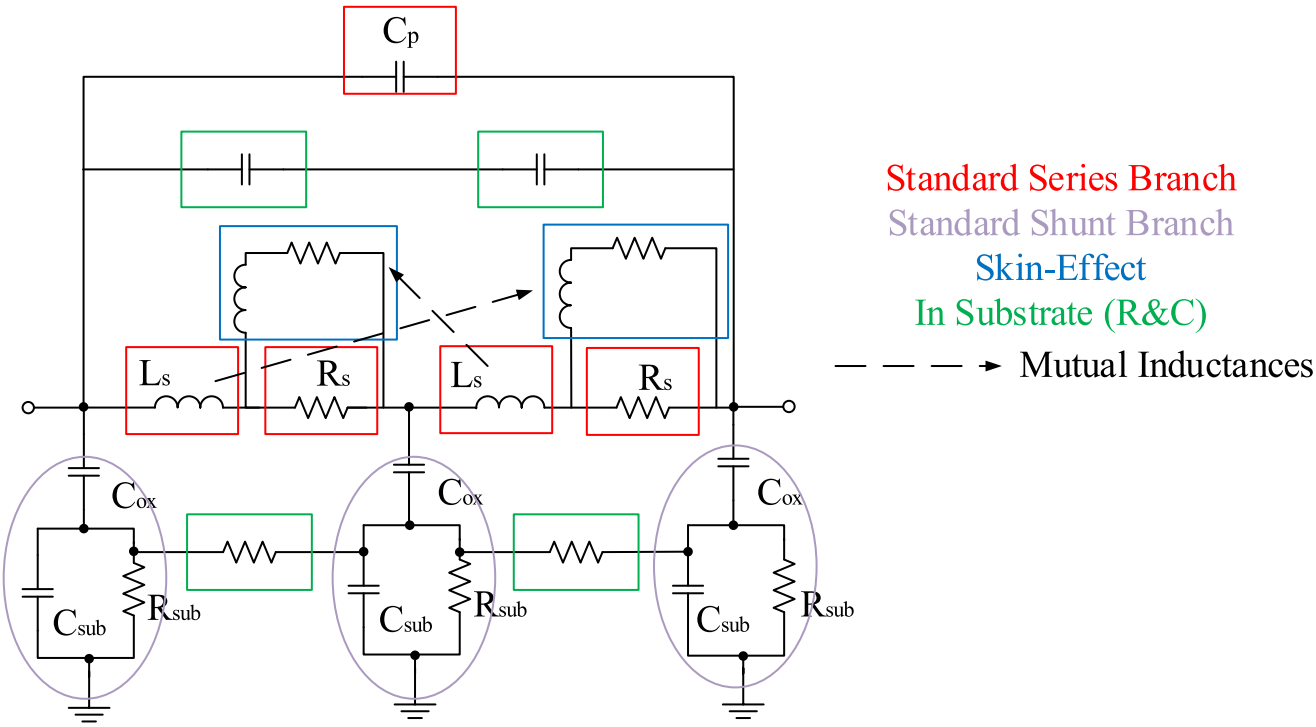


Figure 2.20: The complex model.

a starting point, [47] took the work further by replacing inductors in the series branches with ideal transmission lines and associating each Simple Model with a single turn of the spiral inductor. In [48], Scuderi, Biondi, Ragonese, and Palmisano, presented an "Improved π" topology that is able to model the spiral inductor beyond its Self Resonance Frequency (SRF), which at the time was a improvement into integrated inductor modelling. Xiong and Rustagi introduced a modified version of the π Model in [49] for multi-level spirals. In this work the series branch is modelled with inductively coupled series RL pairs, connected to each other through parallel RC pairs. In March 2003, [50] maintained the simplicity of the π Model by adding a single inductively coupled RL pair to model eddy currents in silicon. In June of the same year, [51] presented the double π version of the same model. It also described the branches of the double π being extracted independently from one another. In December 2003, [52] introduced one of the first asymmetric spiral models. This model is for stacked RFIC spirals and is based on the double π variant of the π model. In the same month, [53] introduced the N-pi version of [52]. The version in [53] uses so-called "N-cells" to model the turns of the spiral. Fig. 2.22 illustrates this topology.

Reference [54] introduced the most complex model presented so far. It is meant to model a three-port differential inductor in a S_iG_e HBT technology. A modified double π with coupling between the inductors in each half was presented in [55]. A modified π Model meant to compensate the ground shielding was proposed in [56]. Kang, Gil and Hyungcheol presented a simplified method for extracting the component values in the skin-effect model in [57]. Reference [58] presented another model which improved the

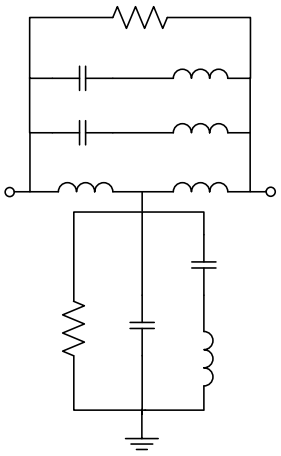


Figure 2.21: Modified T spiral inductor model.

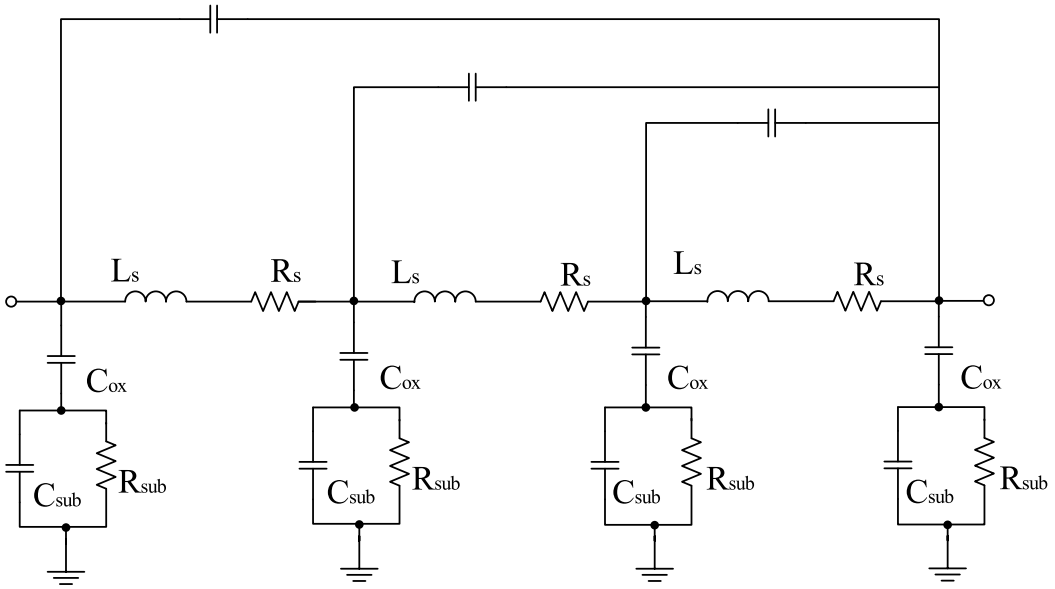


Figure 2.22: Three nested "N-Cells" spiral inductor model.

oxide/substrate modelling of the shunt branches. Lee, Mohammadi, Bhattacharya, and Katehi, in [59] presented an improved Skin-Effect model with third order components effects. Fengyi et al, presented a modified double π model in [60]. Reference [61] presented another variant of the skin-effect model. Wang et al, proposed another asymmetric double π in [62]. Mandal, De, Patra, and Sural proposed another variant of the π Model with improved ground modelling in [63]. Zito, Pepe, and Neri proposed a new shunt branch model with inductance in [64]. Jingxue, Fengyi, and Yusong, in [65], introduce a new double π type model, where the two π sections do not share a shunt branch, but are rather simply cascaded. In 2007, [66], like it was done in [64], introduced inductance into the shunt branch, but for the skin-effect model. A coupled three-port Skin-Effect model was presented in [67]. Reference [68] provided yet another double π model, with a corresponding extraction method. In 2008, a cascaded skin-effect, N-pi model was presented

in [69]. In 2010, a skin-effect model was modified with inductors in the shunt branch. These inductors are coupled to the main inductor in the series branch. An extraction method is provided and the model is shown to work well beyond the SRF.

Despite all the presented models that have already proven its validity, the model developed in this work is based on the basic π model, shown in Fig. 2.16 and based on the work presented on [34] [35]. The objective of this thesis, is to develop a model that is suitable to be used for arbitrary shaped integrated inductors with equal of non-equal turn widths. So this reduces the models that can be used, because the model can only be defined by one series branch, as it will be explained further on. Also, a good complexity-simplicity relationship is desired, so the π model suits the work. It is known that this model has some limitations, that are discussed after the detailed presentation of the model, in Section 3.4.

2.3 Integrated Inductor Advanced Structures

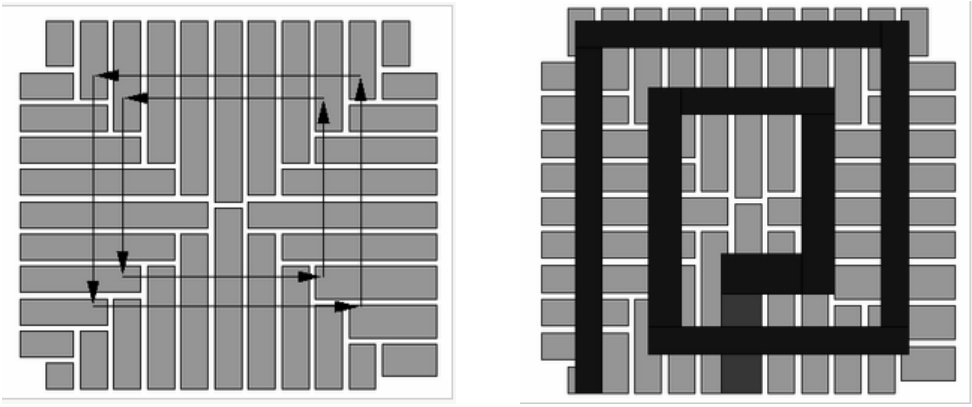
The design of an optimal spiral is highly frequency dependent. This is due to the multiple loss mechanisms that appear from the distributed effects in the structure. In general, for a fixed area, we can design an inductor with many different values of metal width w, spacing s, and turns n, to achieve the same value of inductance. As we increase w for instance, the resistance drops. The substrate losses, though, tend to increase with w, since the increase of w, increases the capacitance of the structure. At the same time, we observe that structures with more turns, n, tend to have higher resistive losses in the inner turns. Besides the effects that geometrical parameters have in the behaviour of integrated inductors, the performance of a typical integrated inductor can be improved with several advanced structures developed through time. Some of these structures are explained in the following sections.

2.3.1 Structures to Reduce Substrate Loss

2.3.1.1 Patterned Ground Shield (PGS)

The substrate loss can be reduced by decreasing the substrate resistance R_{sub}. To achieve this, one can insert a metal or poly-S_i (polycrystalline silicon) layer between the inductor and substrate, and connect this layer to the ground. This approach, called the ground shielding, reduces the effective distance between the spiral metal and ground and thereby reduces the substrate coupling resistance. For a solid ground shield (SGS), however, the varying electromagnetic field in the inductor could induce the eddy current with the presence of ground plane, and the reflected image in the ground plane serves as a counteractive inductor [70]. So it is necessary to pattern the shield as shown in Fig. 2.23 to cut the eddy current loop.

It has been reported that poly-S_i is a good material for the patterned ground shield (PGS) [18]. It was reported in [71] that the use of an n$\pm$ diffusion S_i patterned ground



(a) Substrate with patterned ground shield.

(b) Inductor in a patterned ground shield.

Figure 2.23: Patterned Ground Shield (PGS).

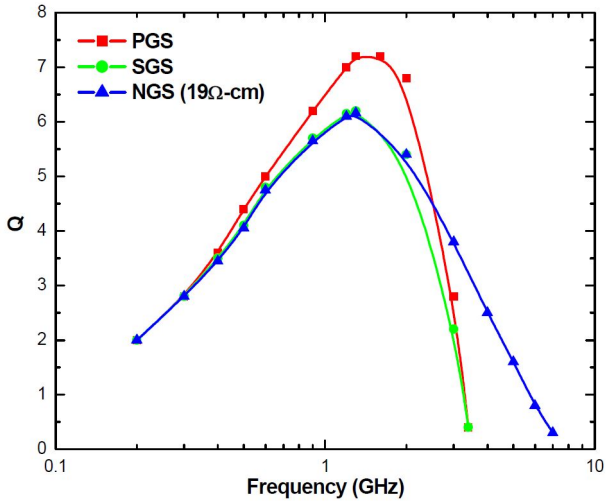
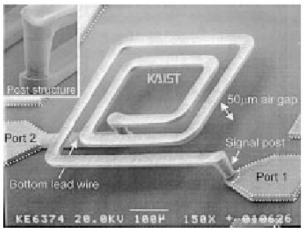
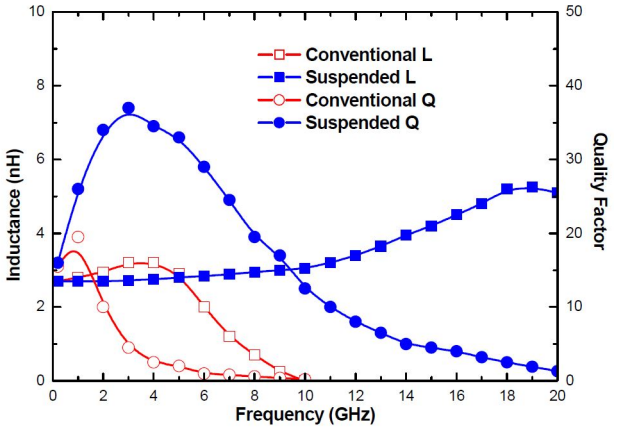


Figure 2.24: Quality factors of solid ground shield (SGS), PGS, and no ground shield (NGS) [4]

shield improves the quality factor in a considerably scale. Since the substrate current mainly concentrates at the S_i-S_iO_2 surface due to the proximity effect, the PGS can effectively break the current loop and thus eliminate the eddy current effect [72]. Fig 2.24 shows the results of quality factor, Q, with SGS and PGS. It is clearly visible that the presence of PGS improves Q considerably. The most significant drawback of ground shielding is the fact that it reduces the distance between inductor and ground and thereby introduces additional capacitances, which adversely decrease the self-resonance frequency [73].



(a) Topology of a suspended inductor.

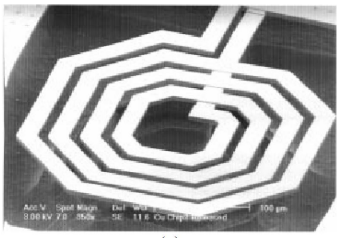


(b) Comparison of inductances and Q factors of conventional and suspended inductors.

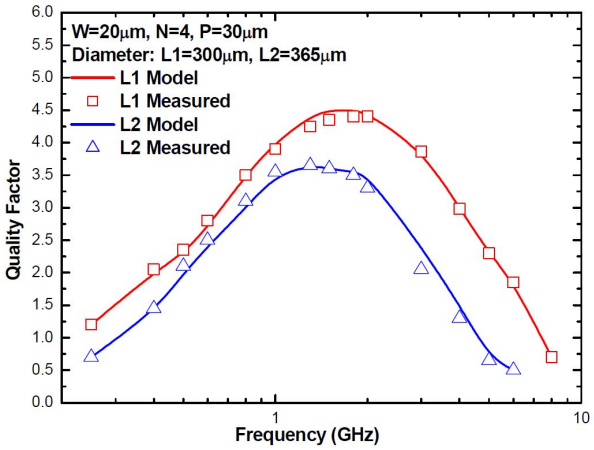
Figure 2.25: Suspended Inductor [5].

2.3.1.2 Substrate Removal

Besides the PGS there is another way to enhance Q, which is to theoretically increase the substrate resistance to $infinite$. A possibility to do this is to use a insulator as substrate. Quartz or glass have proven to achieve better Q and higher self-resonant frequency than S_i substrates [73]. For S_i technology, however, it is not possible to use a high resistive substrate as an effective radio frequency (RF) ground [18]. In other words, for CMOS-based on-chip inductors, it is impossible not to use a low resistive S_i substrate. Nonetheless, instead of building the whole circuit on a low resistive substrate, it is possible to make a region with high resistivity for placing only the inductor [74]. This can be accomplished by using a method called proton implantation [18]. Chan et al. [74] achieved a 7% higher self-resonant frequency and 61% higher Q through this approach. In order to reduce the substrate coupling and losses, researchers have come up with several techniques to keep the inductor away from the substrate. Using an advanced micromachinary process, an inductor can be built above the silicon surface [6], [5] and [75], as shown in Fig. 2.25 and 2.26, or the silicon underneath the inductor can be removed using the deep-trench technology [7], as shown in Fig. 2.27.

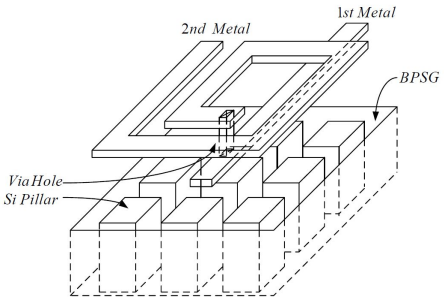


(a) Topology of a micromachined inductor.

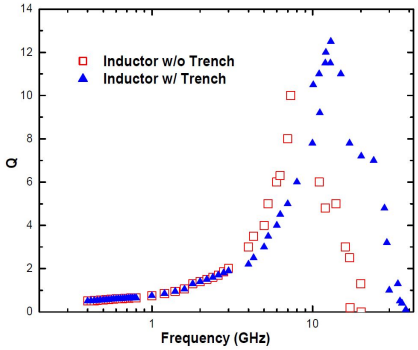


(b) Q factors of micromachined inductors with two different diameters.

Figure 2.26: Micromachined inductor [6].



(a) Inductor with substrate removed by a deep trench technology.

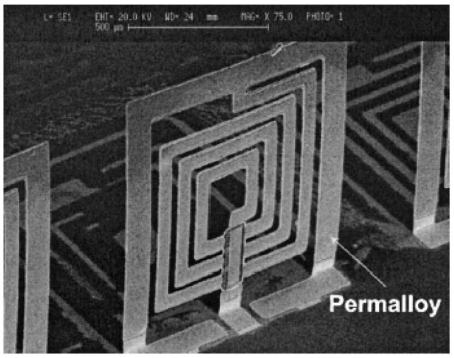


(b) Q factors of conventional and trenched inductors.

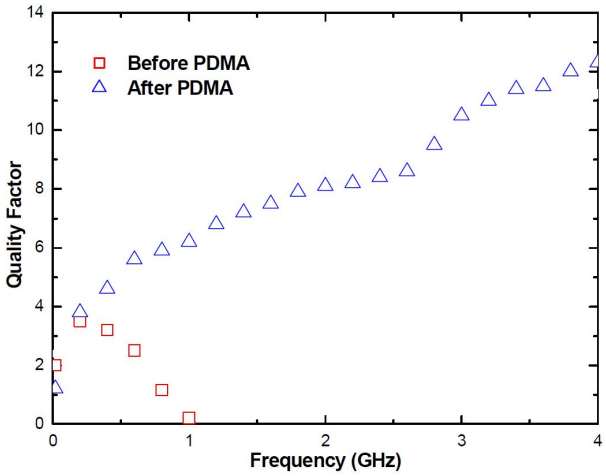
Figure 2.27: Inductor with substrate removed technology [7].

2.3.1.3 Horizontal Inductors

Another way to reduce the substrate losses is to reduce the magnetic field coupling to substrate. This can be obtained by having the magnetic field parallel to the substrate. Research works have been studying the possibility to fabricate horizontal inductors with multilayer interconnections [76] [77]. By using this technique, the magnetic field is parallel to the substrate surface and the magnetic coupling to the substrate is minimal. However this structure increases the coupling capacitance. Since a large metal is needed for the bottom layer of the horizontal inductor, the inductor-substrate capacitance increases tremendously if the inductor is on silicon. Again, researchers tried to use high resistive substrate [77], and suspended the inductor in air [78], or even rectify the inductor with the so-called plastic deformation magnetic assembly (PDMA) [8]. Fig. 2.28 shows the topology and performance of a horizontal inductor using the PDMA.



(a) Topology of the horizontal inductor based on the PDMA process.



(b) Q factors of conventional and horizontal inductors.

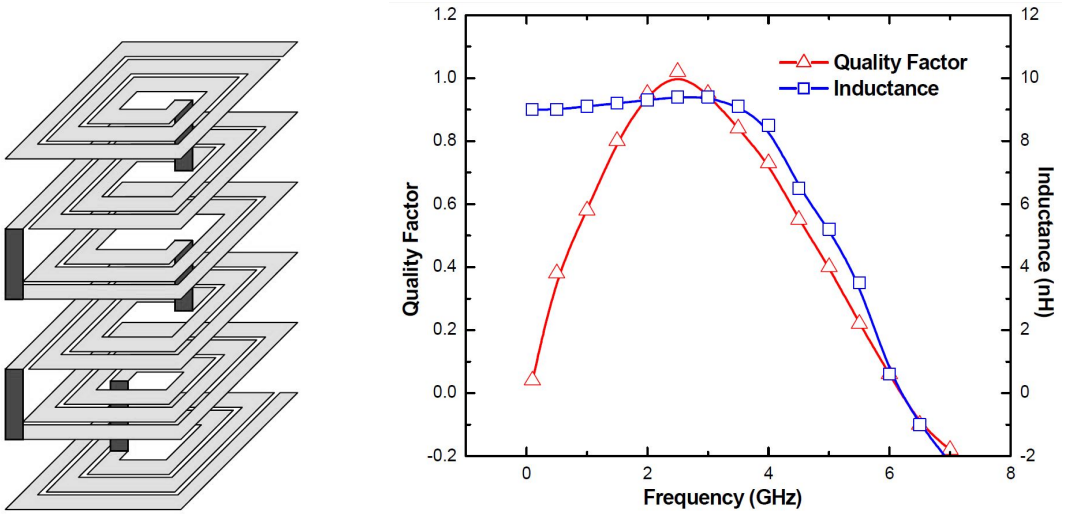
Figure 2.28: Horizontal integrated inductor based on the PDMA [8].

2.3.2 Structures to Increase Inductance

Since the quality factor is directly proportional to the series inductance, approaches to increase the inductance have also been suggested for on-chip inductor performance enhancement.

2.3.2.1 Stacked Inductor

A stacked inductor is a set of series inductors made from different metal layers, as illustrated in Fig. 2.29. This method maximizes the inductance per unit area. It has been reported that a 10 nH inductor can be achieved with an area of 22 $\mu m^2 \sim 23\ \mu m^2$, as opposed to several hundreds μm^2 for regular inductors [9]. This is the main advantage that this technology can offer. The biggest drawbacks are the relatively low Q factor and self-resonant frequency, due to the increase of the substrate capacitance and line to line coupling capacitance. The Q factor and inductance of such an inductor are illustrated in Fig. 2.29.



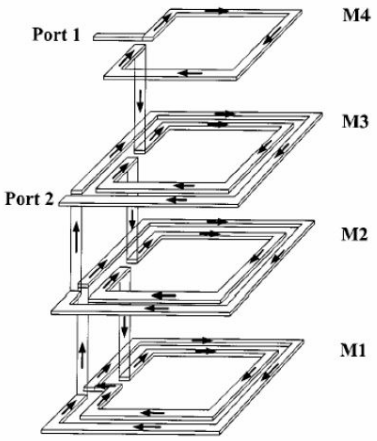
(a) Stacked inductor with six metal layers.

(b) Q factors of conventional and horizontal inductors.

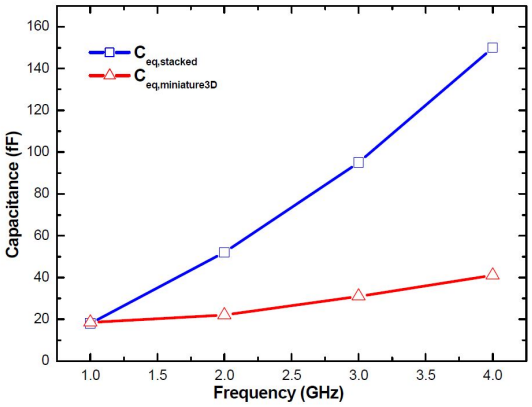
Figure 2.29: Q factor and inductance of the stacked inductor [9].

2.3.2.2 Miniature 3-D Inductor

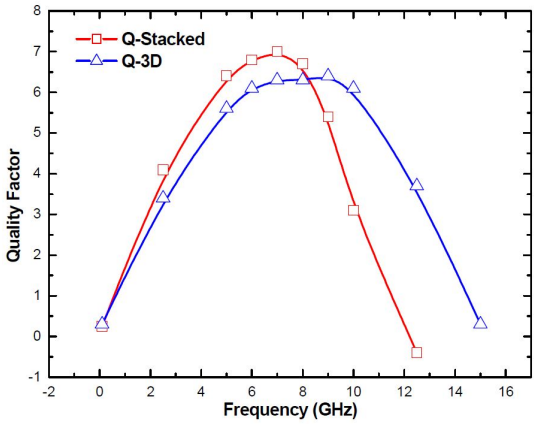
A high-performance stack-like inductor, called the miniature 3-D inductor, was proposed in [10]. Fig. 2.30(a) shows such an inductor, which consists of at least two or more stacked inductors by series connections, and every stacked inductor has only one turn in every metal layer. The miniature inductor, while quite complicated, possesses a minimal coupling capacitance. This leads to a much higher self-resonant frequency and a wider frequency range for high quality factor. Comparisons of capacitances and Q factors obtained from this inductor and a typical stacked inductor are also given in Fig. 2.30(b) and 2.30(c).



(a) Structure of the miniature 3-D inductor.



(b) Capacitances of typical stacked and 3-D inductors,.



(c) Q factors of typical stacked and 3-D inductors.

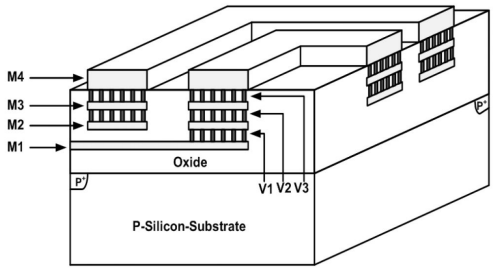
Figure 2.30: Miniature 3-D inductor [10].

2.3.3 Structures to Reduce Series Resistance

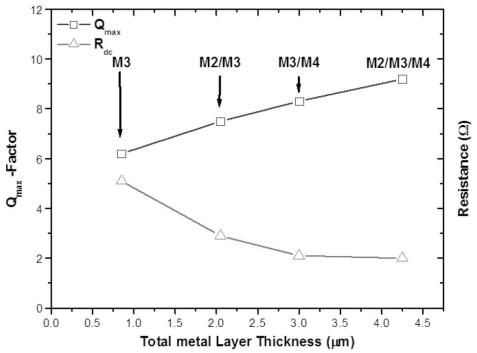
Metal resistivity gives rise to the series resistance R_s, and it is always desired to reduce the resistance in order to improve the quality factor. One simple idea is to increase the line width. This method may work at low frequencies where the current density in a wire is uniform; however, as the frequency increases, the skin effect pushes more current to the outer cross section of the metal wire and the so-called skin depth (i.e., the depth in which the current flows) is reduced with increasing frequency (see Eq. 2.8). Thus, the skin effect increases the series resistance at high frequencies, and the approach of increasing the line width would not be effective. According to an earlier study, the larger the cross section, the lower the onset frequency at which the skin effect dominates the series resistance. Furthermore, a wider metal line would occupy more area, which increases the fabrication cost. Several possible solutions to this problem are given below.

2.3.3.1 Vertical Shunt

In this approach, the inductor is made of multiple metal layers and the neighboring metal layers are shunted through via arrays, so the effective thickness of the spiral inductor is increased, the skin effect is weakened, and the series resistance is reduced. A detailed study and comparison on the multilayer inductors are presented in [11].



(a) Inductor with multiple metal layers and vertical shunt.



(b) Maximum Q factors and resistances for the inductor having different numbers of vertical shunt.

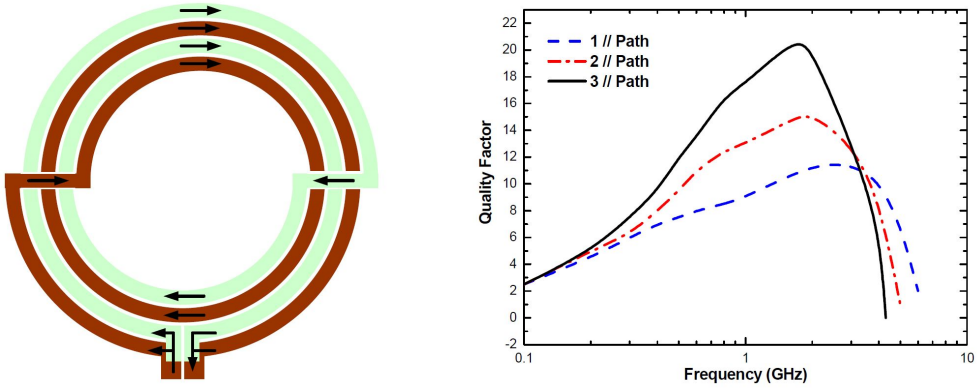
Figure 2.31: Vertical shunt integrated inductor [11].

The inductors are fabricated with multiple metal layers (M1 to M4). These layers can be shunted through via arrays, as shown in Fig. 2.31 for the case of shunting M2, M3 and M4. The results in Fig. 2.31 show a reduced series resistance and thus an improved Q as the number of shunts is increased (i.e., the case of M3 has no vertical shunt). The performance of the inductor is therefore optimized with the increment of total metal thickness without occupying more area. One important aspect the inductor in Fig. 2.31 did not address is that the inductor may experience a lower self-resonant frequency with the utilization of lower metal layers. This is due to the following effects:

- The reduction of metal-substrate distance could cause a significant increase in C_{ox},
- The capacitance among the metal lines would also increase.

2.3.3.2 Horizontal Shunt

Instead of shunting vertically, the spiral inductor can be split into several shunting current paths, each with an identical resistance and inductance. This approach, called the horizontal shunt, can suppress the current crowding and increase the Q factor [12]. Figs. 2.32 show such an inductor and its Q factor. It is shown that for the same line width, the Q factor increases with increasing number of splits.



(a) Inductor with metal line split into shunt current paths.

(b) Q factors of horizontally shunt inductor with one, two, and three splits in the metal line.

Figure 2.32: Horizontal shunt inductor [12].

2.3.3.3 Variable Width Inductors

For inductors fabricated with a constant line width, the influence of magnetically induced losses is much more significant in the inner turns of the spiral, where the magnetic field reaches its maximum. For this reason hollow spirals are preferred [79]. The origin of these magnetic losses stems from the fact that the magnetic flux increases as we move towards the center of the spiral, due to the additive nature of the flux from each successive loop of the spiral. If the width of the structure is tapered, as shown in Fig. 2.34, then the

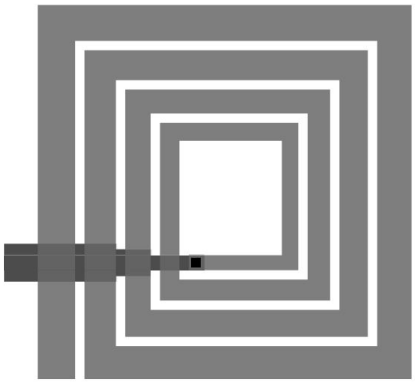


Figure 2.33: A square spiral inductor with tapered trace width.

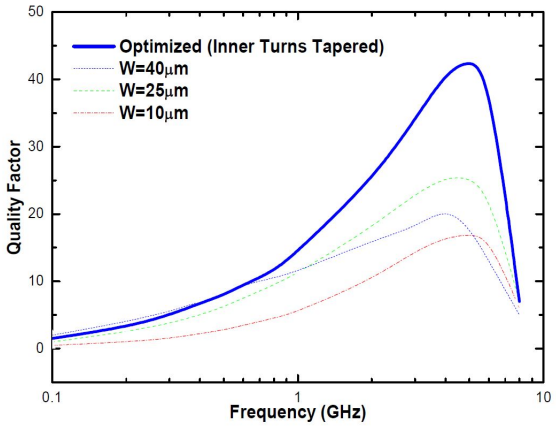


Figure 2.34: Q factors of a tapered inductor and three non-tapered inductors [13].

performance of the spiral can be improved. Since the wide inner turns do not lower the resistance (due to current constriction), it is better to transfer the width to the outer turns, while keeping the total area of the spiral constant.

Detailed study was performed in [13] regarding the optimization of line width in order to enhance the RF performance. The frequency and position-dependent optimum width W_{opt} is given by:

$$W_{opt,n} = \sqrt[3]{\frac{r_s(f)}{2 \cdot C \cdot g_n^2 \cdot f^2}} \tag{2.12}$$

where $r_s(f)$ is the sheet resistance of the metal strip, f is the frequency, C is a fitting constant, and g_n is a geometric dependent parameter. As can be seen in Fig. 23(b), the Q factor of a spiral inductor is much improved when the line width is not uniform and is optimized.

3

Analytical Modelling of Integrated Inductors

In this chapter the developed model will be explained. The model is based in the usually called segmented model, due to the fact that the inductors are divided into segments. The analytical expressions for each lumped element will be presented and its physical definition will be given.

3.1 Segmented Model and its Analytical Expressions

Considering a one-turn square inductor, the idea is to divide the inductor into four segments, as shown in Fig. 3.1. Afterwards, a π lumped element circuit is used to model each segment of the integrated inductor. The π model, shown in Fig. 2.16, was introduced in the previous chapter but a detailed explanation of its elements will be given in this chapter.

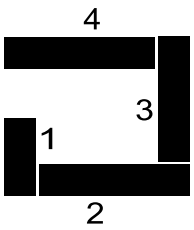


Figure 3.1: Inductor model description for a one-turn inductor.

In Fig. 3.2 it is possible to observe how this model works in every stage, first the

trimming into different segments and afterwards the usage of lumped-elements to characterize the inductor. At the final stage of the modelling one should have a circuit like the one shown in Fig. 3.3. For the sake of simplicity, when using a SPICE-like simulator it is possible to sum each one of the lumped element of each segment, this way we will have just one equivalent schematic, which will speed up the inductor design.

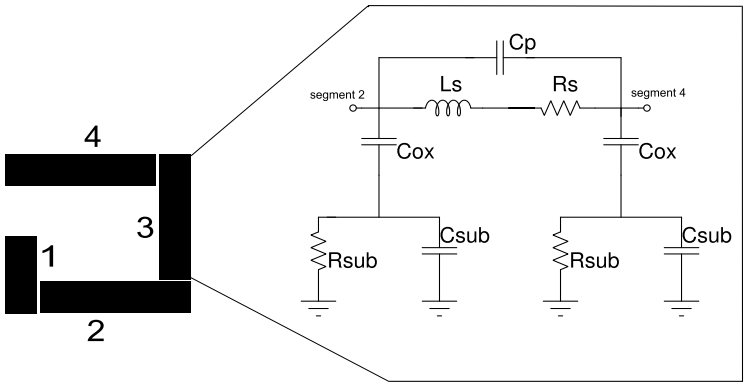


Figure 3.2: Model explanation with an inductor trimmed and the π model.

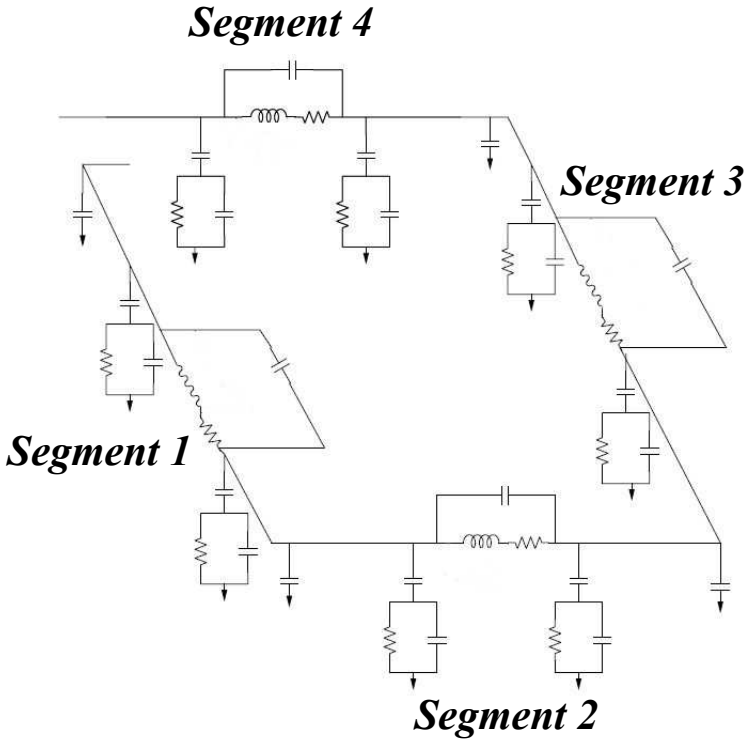


Figure 3.3: One-turn integrated inductor defined by the segment model.

The series branch of this model, consists of L_s, R_s and C_p. The series resistance, R_s arises from metal resistivity of the inductor and is closely related to the quality factor, being a key issue for inductor modelling. The series feedforward capacitance, C_p, has usually been considered as the overlap capacitance between the spirals and the underpass metal lines, also called C_o and showed in Fig. 3.4. However, as the minimum feature

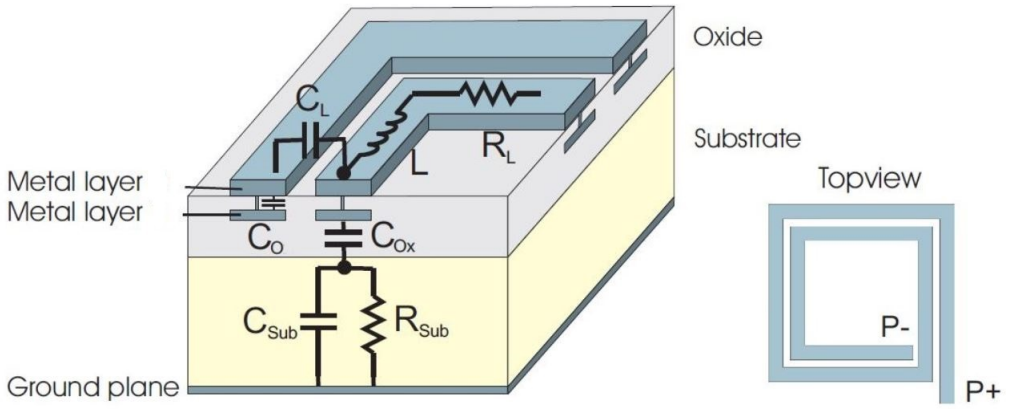


Figure 3.4: Physical definition of the lumped-elements of the inductor model.

size of CMOS process continues to shrink, the spacing between metal spirals, s, can be reduced to a value similar to the distance to the underpass. Therefore the coupling capacitance between metal lines, C_L, can play a major role in the total capacitance of the device, and therefore in the self resonance frequency (SRF). C_p is then given by the sum of C_s and C_o. The capacitance C_{ox} represents the oxide capacitance between the spiral and the substrate. The silicon substrate is modelled with C_{sub} and R_{sub} [80] [30] [81] [18].

$$R_s = k \cdot \frac{\rho \cdot l}{w \cdot \delta \cdot (1 - e^{-t/\delta})} \tag{3.1}$$

$$C_{ox} = \frac{1}{2} \cdot l \cdot w \cdot \frac{\varepsilon_{ox}}{t_{ox}} \tag{3.2}$$

$$R_{sub} = \frac{2}{l \cdot w \cdot G_{Sub}} \tag{3.3}$$

$$C_{sub} = \frac{1}{2} \cdot l \cdot w \cdot C_{ms} \tag{3.4}$$

$$C_o = n \cdot w^2 \cdot \frac{\varepsilon_{ox}}{t_{M1-M2}} \tag{3.5}$$

Eq. 3.1 to Eq. 3.5 define the π model for an integrated inductor on silicon. However, as it was mentioned previously, with the continuing shrinking size of CMOS and with higher operating frequency, s will get smaller and the parasitic capacitances will affect inductors more significantly. In Eq. 3.1, k is a fitting factor.

To use this model up to higher frequency range, the capacitance C_L must be taken into account and C_{ox} and C_{sub} should be calculated using different methods that include high frequency effects such as the skin and proximity effects. The distributed capacitance model (DCM) is one of those methods [82]. The fundamental assumptions of DCM can be derived from the voltage distribution over the inductor, which is called voltage profile

[83]. For the sake of simplicity the following assumptions should be made.

1. The wiring metal width should be much larger than the spacing.
2. Voltage distribution is proportional to the lengths of the metal tracks, i.e., if the metal track is longer, the voltage drop on the track is higher.
3. In the same turn, the voltage is regarded as constant and it is determined by averaging the beginning voltage and the ending voltage of the turn.

To calculate the capacitances, we first define the lengths of each segment as l_1, l_2,..., l_n, and the total length as l_{tot}=l_1+l_2+...+l_n, where l_n is the length of the last segment of the outer turn. Afterwards we define,

$$h_k = \sum_{k=1}^{n} \frac{l_k}{l_{tot}} \tag{3.6}$$

and the capacitances can be calculated with the following formulas [82],

$$C_s = \sum_{k=1}^{n} x \cdot \frac{4}{3} C_{mm} l_k \cdot \frac{\left[(h_k - h_{k-1})^2 + (h_{k+1} - h_k)^2 + (h_{k+1} - h_k)(h_k - h_{k-1})\right]}{(h_{k+1} - h_{k-1})^2} \tag{3.7}$$

$$C_{ox} = \sum_{k=1}^{n} x \cdot \frac{1}{2} \cdot \frac{4}{3} C_{ms} l_k \cdot \frac{\left[(1 - h_{k-1})^2 + (1 - h_k)^2 + (1 - h_k)(1 - h_{k-1})\right]}{3(2 - h_k - h_{k-1})^2} \tag{3.8}$$

An empirical scale factor x, which is the same for both equations, of the total C_p capacitance for each segment is shown to match the distributed capacitance for simulations over a wide range of physical parameters and layouts. This empirical capacitance factor is then used as a fitting parameter to the measured SRF and Q over a large set of inductors.

The $1/2$ factor in C_{ox}, is due to the fact that the capacitance is divided into two in the π-model. C_{mm} and C_{ms}, are the unit length capacitance between the metal spirals and the unit length capacitance between the metal and the substrate, respectively. Normally these are extracted from measured data, but they can be approximated as follows [84],

$$C_{mm} = \frac{\varepsilon_0 \varepsilon_{s_i O_2} \cdot t}{s} \tag{3.9}$$

$$C_{ms} = \frac{\varepsilon_0 \varepsilon_{s_i O_2} \cdot w}{h_{s_i O_2}} \tag{3.10}$$

where ε_0 is the vacuum permittivity and $\varepsilon_{s_i O_2}$ is the relative permittivity. $h_{s_i O_2}$ is the distance from the metal to substrate.

The substrate resistance is crucial for accurately modelling of the peak Q and the shape of the Q curve, along with the series resistance R_s. This resistance can be calculated by Eq. 3.11, given in [18] and [30],

$$R_{sub} = \frac{2}{l \cdot w \cdot G_{sub}} \tag{3.11}$$

where l is the segment length and G_{sub} is the conductance per unit area for the silicon substrate and can be approximated according to [84] by,

$$G_{sub} = \frac{\sigma_{si}}{h_{S_i}} \tag{3.12}$$

where σ_{S_i} is the conductivity of the silicon substrate and h_{S_i} is the thickness of the substrate.

The substrate capacitance can normally be approximated using a simple fringing capacitance model as the one given in [30]. However, to extend our model to high frequencies with more accuracy, we use the DCM model technique to calculate the substrate capacitance, as shown in Eq. 3.13 [82].

$$C_{sub} = \sum_{k=1}^{n} x \cdot \frac{1}{2} \cdot \frac{4}{3} C_{ss} l_k \cdot \frac{\left[(1-h_{k-1})^2 + (1-h_k)^2 + (1-h_k)(1-h_{k-1})\right]}{3(2-h_k-h_{k-1})^2} \tag{3.13}$$

Again, x is the same fitting factor used for previous equations, the $1/2$ factor in C_{sub}, is due to the fact that the capacitance is divided into two in the π-model and C_{ss} is the length capacitance between the substrate and the ground plane, which can be approximated by the following equation [84],

$$C_{ss} = \frac{\varepsilon_0 \varepsilon_{s_i} \cdot w}{h_{S_i}} \tag{3.14}$$

The inductance L_s represents the series inductance and can be calculated through several given formulas and techniques.

- **Greenhouse method** - This method offers sufficient accuracy and adequate speed, but cannot provide an inductor design directly. The formula for the inductance value is given by equation 3.22.

$$L = 2l \left\{ ln \left[\frac{2l}{w+t} \right] + 0.50049 + \frac{w+t}{3l} \right\} (nH) \tag{3.15}$$

- **Modified Wheeler Formula** - Wheeler presented several formulas for planar spiral inductors [85]. Mohan [86] discovered that a simple modification of the formula would also allowed it to be used for planar spiral integrated inductors. Some physical definitions are needed to understand the formulas, such as the average diameter

D_{avg} = 0.5(D_{out} + D_{in}) or the fill ratio, defined as ρ = (D_{out} - D_{in})/(D_{out} + D_{in}),

$$L = K_1 \mu_0 \frac{n^2 d_{avg}}{1 + k_2 \rho} \tag{3.16}$$

where ρ is the fill ratio defined previously and the coefficients K_1 and K_2 depend on the geometry and are shown in Table 3.1.

Layout	K_1	K_2
Square	2.34	2.75
Hexagonal	2.33	3.82
Octagonal	2.25	3.55

Table 3.1: Coefficients for modified Wheeler expression.

- **Expression Based on Current Sheet Approximation** - Another simple yet accurate expression for the inductance of a planar spiral can be obtained by approximating the sides of the spirals by symmetrical current sheets of equivalent densities [87].

$$L = \frac{\mu_0 n^2 d_{avg} c_1}{2} (ln(c_2/\rho) + c_3 \rho + c_4 \rho^2) \tag{3.17}$$

where coefficients c_i are layout dependent and are shown in Table 3.2.

Layout	c_1	c_2	c_3	c_4
Square	1.27	2.07	0.18	0.13
Hexagonal	1.09	2.23	0.00	0.17
Octagonal	1.07	2.29	0.00	0.19
Circle	1.00	2.46	0.00	0.20

Table 3.2: Coefficients for current sheet expression.

- **Data Fitted Monomial Expression** - This method is based on a data fitting technique, which yielded the expression,

$$L = \beta d_{out}^{\alpha_1} w^{\alpha_2} d_{avg}^{\alpha_3} n^{\alpha_4} s^{\alpha_5} \tag{3.18}$$

where the coefficients β and α_i are layout dependent and given in table 3.3.

Layout	β	α_1	α_2	α_3	α_4	α_5
Square	$1.62 \cdot 10^{-3}$	-1.21	-0.147	2.40	1.78	-0.030
Hexagonal	$1.28 \cdot 10^{-3}$	-1.24	-0.174	2.47	1.77	-0.049
Octagonal	$1.33 \cdot 10^{-3}$	-1.21	-0.163	2.43	1.75	-0.049

Table 3.3: Coefficients for data fitted monomial expression.

However, the techniques presented above only provide the means to calculate the series inductance for previously studied layouts. The main focus of this work is to determine analythical expressions for the evaluation of the series inductance, L_s, for integrated planar tapered inductors of any shape (square, hexagonal, octagonal), as a way of providing more physical insights into the design key parameters [18].

In 1929, Grover derived formulas for inductance calculation between filaments in several different positions [88]. Greenhouse later applied these formulas to calculate the inductance of a square shaped inductor by dividing the inductor into straight-line segments, as ilustrated in Fig. 3.1, and evaluating the inductance by adding up the self inductance of the individual segment and mutual inductance between segments [89]. Some authors call this method the $mutual\ inductance\ approach$ [2]. For the inductor depicted in Fig. 3.1, the series inductance is given by Eq. 3.19. This specific case is the least complex one, where there are no mutual inductances between segments.

$$L_s = L_1 + L_2 + L_3 + L_4 \tag{3.19}$$

In the next sections, a more detailed explanation will be given on how to calculate the series inductance for several integrated inductors layout.

3.2 Square Inductor Series Inductance Calculation

For the general case of an n-turn inductor as depicted in Fig. 3.5, it is possible to calculate the series inductance of the inductor, by Eq. 3.20.

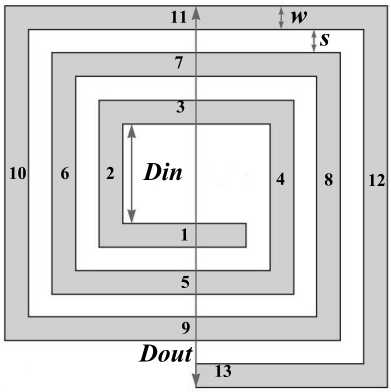


Figure 3.5: Thirteen section square spiral inductor layout.

$$L_s = L_0 + M_{p+} - M_{p-} \tag{3.20}$$

where L_s is the total series inductance of the inductor, L_0 is the self inductance of each segment, M_{p+} is the mutual inductance where the current flows in the same direction whereas M_{p-} accounts for mutual inductance of the parallel segments where currents flow in the opposite directions [90]. This formula was proposed by Greenhouse and

suitable for square inductors. In the next sections we present an analytical method to calculate the inductance of integrated inductor with any shape, such as hexagonal or octagonal. Furthermore, the characterization of tapered inductors of any shape may be obtained in a straightforward way. For the example given in Fig. 3.5 it is possible to calculate the L_s value through Eq. 3.21. Due to the magnitude and phase of the currents, these are assumed identical in all sections, so $M_{a,b}$=$M_{b,a}$, yielding,

$$\begin{aligned} L_s = {} & L_1 + L_2 + ... + L_{13} \\ & \text{(Self inductance)} \\ & + 2(M_{1,5} + M_{2,6} + M_{3,7} + M_{4,8} + M_{5,9} + M_{6,10} + M_{1,9} + ... + M_{8,12}) \\ & \text{(Positive mutual inductances)} \\ & - 2(M_{1,7} + M_{1,3} + M_{2,8} + M_{2,4} + M_{3,9} + M_{3,5} + ... + M_{1,11}) \\ & \text{(Negative mutual inductances)} \end{aligned} \tag{3.21}$$

In order to calculate the self inductance the Greenhouse formula given in [89] may be applied, where

$$L = 2l \left\{ ln \left[\frac{2l}{w+t} \right] + 0.50049 + \frac{w+t}{3l} \right\} (nH) \tag{3.22}$$

where L is the segment inductance in nanohenries and w and t come in centimetres. These units are explained in [89]. For the evaluation of the mutual inductances the formulas deducted by Groover [88] may be applied. For the case of two parallel segments as depicted in Fig. 3.6, the formula used to calculate mutual inductance is given by Eq. 3.23, where l and m represent the segments lengths, d the distance between them, and p and q represent the difference between the length of the segments.

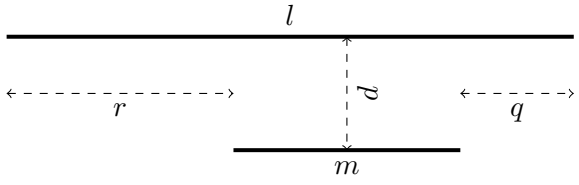


Figure 3.6: Parallel segments.

$$2M = (M_{m+r} + M_{m+q}) - (M_r + M_q) \tag{3.23}$$

Given that each $M_{i,j}$ is calculated with the following formula,

$$M = 2 \cdot l \cdot U \tag{3.24}$$

where the mutual inductance, U, is calculated by Eq. 3.25.

$$U = ln\left[\frac{l}{d} + \sqrt{1 + \left(\frac{l}{d}\right)^2}\right] - \sqrt{1 + \left(\frac{d}{l}\right)^2} + \frac{d}{l} \tag{3.25}$$

Given that the distance between segments, d, is considered as the geometric mean distance (GMD) between segments and calculated by Eq. 3.26,

$$lnGMD = lnp - \frac{w^2}{12p^2} - \frac{w^4}{60p^4} - \frac{w^6}{168p^6} - \frac{w^8}{360p^8} - \frac{w^{10}}{660p^{10}} - \cdots \tag{3.26}$$

where, p is the pitch of the two wires and w is the width of the segments in study. Note that, for the particular case of a square inductor, the series inductance calculation will not comprise the mutual inductance between two consecutive segments, since their mutual inductance is zero.

3.3 N-Side Inductor Series Inductance Calculation

The series inductance calculation of non-square inductors is more complex [18] due to the necessity of evaluating mutual inductances between non-parallel segments. In this section the evaluation of the series inductance, L_s, for an octagonal inductor will be given as an example. Further generalization of the formula for an n-side inductor is also addressed. For hexagonal layouts the angle between segments is 120 degrees, and for octagonal layouts the angle is 135 degrees and so on. For N-side layouts, with N being bigger than four, and with the new mutual inductances appearing, Eq. 3.20 must be replaced by Eq. 3.27.

$$L_s = L_0 + M_{p+} - M_{p-} - M_{lm} \tag{3.27}$$

Where M_{lm} accounts for all the different types of mutual inductances resulting from non-parallel segments. These mutual inductances should be summed or subtracted depending on the flow of the current.

For the particular case of the inductor in Fig. 3.7 it is possible to calculate the L_s value through Eq. 3.28. Again, due to the magnitude and phase of the currents, the mutual inductances are assumed identical in all sections, hence $M_{a,b}$=$M_{b,a}$.

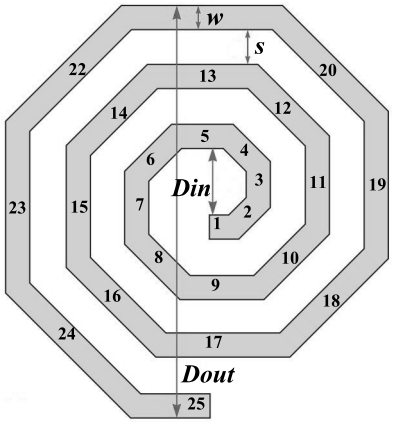


Figure 3.7: Twenty-five section octagonal spiral inductor layout.

$$
\begin{aligned}
L_s = {} & L_1 + L_2 + ... + L_{25} \\
& \text{(Self inductance)} \\
& + 2(M_{1,9} + M_{2,10} + M_{3,11} + M_{4,12} + M_{5,13} + M_{6,14} + ... + M_{17,25}) \\
& \text{(Positive mutual inductances)} \\
& - 2(M_{1,5} + M_{2,6} + M_{3,7} + M_{4,8} + M_{5,9} + M_{10,6} + ... + M_{25,21}) \\
& \text{(Negative mutual inductances)} \\
& - 2(M_{1,2} + M_{2,3} + M_{24,25} + ... + M_{1,3} + M_{3,5} + M_{23,25} + \\
& ... + M_{1,11} + M_{2,12} + ... + M_{16,25}) \\
& \text{(Mutual inductances as shown in Fig. 3.8 - 3.11)}
\end{aligned}
\tag{3.28}
$$

An example for mutual inductance for segments which are connected at one end, such as $M_{4,3}$, is present in Fig. 3.8.

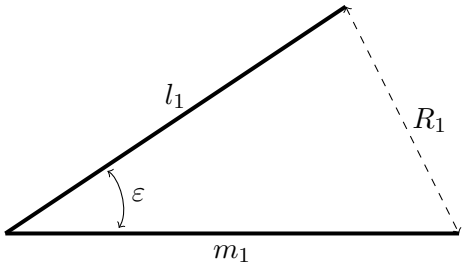


Figure 3.8: Segments which are connected at one end.

These type of mutual inductance are calculated through Eq. 3.29 [88].

$$
M_{lm} = 2cos\varepsilon \left[l_1 tanh^{-1}\left(\frac{m_1}{l_1 + R_1}\right) + m_1 tanh^{-1}\left(\frac{l_1}{m_1 + R_1}\right)\right] \tag{3.29}
$$

In Eq. 3.29, l_1 and m_1 are the lengths of the segments and R_1 is the distance between the segment ends, and can be calculated by Eq. 3.30.

$$R_1^2 = 2l^2(l - cos\varepsilon) \tag{3.30}$$

It is also possible to use one of the following relations to substitute either R_1 or ε.

$$cos\varepsilon = \frac{l^2 + m^2 - R_1^2}{2lm} \tag{3.31}$$

$$\frac{R_1^2}{l^2} = 1 + \frac{m^2}{l^2} - 2\frac{m}{l}cos\varepsilon \tag{3.32}$$

The case of mutual inductance where the intersection point is lying outside the two filaments, for example, $M_{3,5}$, is given in Fig. 3.9. Whereas the case where the intersection point lies upon one filament, which is the most complex case, such as $M_{5,14}$, is presented in Fig. 3.10.

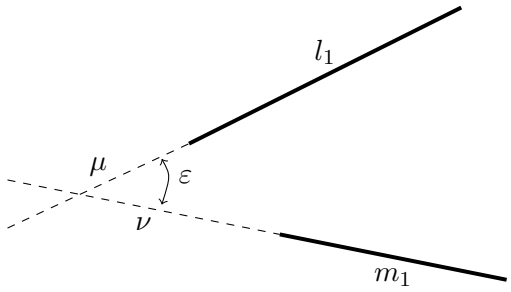


Figure 3.9: Case for when the intersection point is lying outside the two filaments.

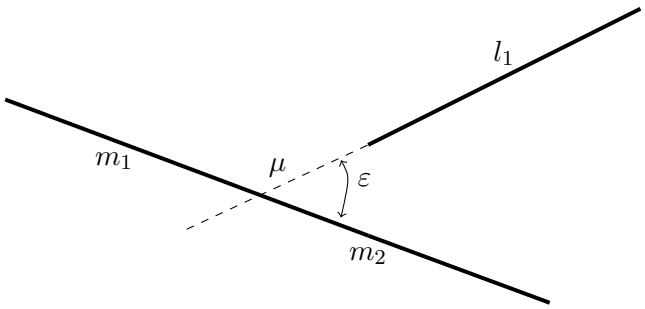


Figure 3.10: Case for when the intersection point lies upon one filament.

The mutual inductances in Fig. 3.9 and Fig. 3.10 are calculated by the following equation,

$$M_{lm} = 2cos\varphi\left[(M_{\mu+l,\nu+m} + M_{\mu\nu}) - (M_{\mu+l,\nu} - M_{\nu+m,\mu})\right] \tag{3.33}$$

The general case for mutual inductances between segments is given in Fig. 3.11. Further we present a series of formulas used to calculate the mutual inductances between unequal segments at the same plane [88].

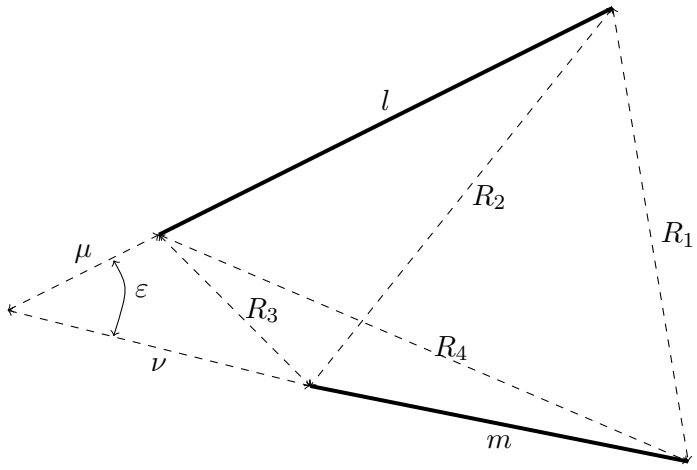


Figure 3.11: General case for two segments placed in the same plane.

$$2cos\varepsilon = \frac{\alpha^2}{lm} \tag{3.34}$$

$$\alpha^2 = R_4^2 - R_3^2 + R_2^2 - R_1^2 \tag{3.35}$$

$$\mu = \frac{l\left[2m^2(R_2^2 - R_3^2 - l^2) + \alpha^2(R_4^2 - R_3^2 - m^2)\right]}{4l^2m^2 - \alpha^2} \tag{3.36}$$

$$\nu = \frac{m\left[2l^2(R_4^2 - R_3^2 - m^2) + \alpha^2(R_2^2 - R_3^2 - l^2)\right]}{4l^2m^2 - \alpha^2} \tag{3.37}$$

$$R_1^2 = (\mu + l)^2 + (\nu + m)^2 - 2(\mu + l)(\nu + m)cos\varepsilon \tag{3.38}$$

$$R_2^2 = (\mu + l)^2 + \nu^2 - 2\nu(\mu + l)cos\varepsilon \tag{3.39}$$

$$R_3^2 = (\mu)^2 + \nu^2 - 2\nu\mu cos\varepsilon \tag{3.40}$$

$$R_4^2 = (\mu)^2 + (m + \nu)^2 - 2\mu(\nu + m)cos\varepsilon \tag{3.41}$$

And at last, after calculating the intermediary geometric parameters R_1 to R_4, the mutual inductance is calculated with the following equation.

$$M_{lm} = 2cos\varepsilon \cdot \left[(\mu + l) \cdot tanh^{-1}\left(\frac{m}{R_1 + R_2}\right) + (\nu + m) \cdot tanh^{-1}\left(\frac{l}{R_1 + R_4}\right) - \mu \cdot tanh^{-1}\left(\frac{m}{R_3 + R_4}\right) - \nu \cdot tanh^{-1}\left(\frac{l}{R_2 + R_3}\right) \right] \quad (3.42)$$

Using Eq. 3.34-3.41 and Eq. 3.42, the inductance of any piecewise structure can be approximated. Given enough segments and a modern workstation any smooth curve can be obtained. However it is easy to understand that when one increases the number of segments the difficulty of calculation increases exponentially due to the number of new mutual inductances that appear [2].

3.4 Model Simplifications and Limits

The common π-model has proven its validity up to 1 GHz in already presented works [4] [30]. The objective of this thesis is to develop a new model, based on the π-model, that can be used at higher frequencies and can also be used into an optimization tool. The main objective is that the model achieves accurate results at 2.4 GHz. This frequency was chosen because it is the industrial, scientific and medical (ISM) radio band. These bands are mostly used for short-range, low power communications systems, such as, cordless phones, Bluetooth devices, near field communication (NFC) devices, and wireless computer networks. The π-model was developed with certain approximations that will reflect some limitations in the validity of the model for certain regions, these approximations are either by lack of elements or the approximated equations used to model the elements. Due to this fact, the model has to be used according to these limiting factors.

However, the model developed already takes into account the skin effect in the series resistance equation [30], and the proximity effect in the capacitance model (DCM) [82], which is an improvement from the common π-model presented in [4].

Besides the already modelled effects, there is an important factor in integrated inductors which is not considered in the model, the Eddy currents. This will bring some restrictions on the physical parameters of the inductors, such as the D_{in}.

Another physical restriction is the turn width, w. When the turn width increases, the GMD value, turns to be a less accurate method to calculate the distance between points in each turn. Also, when the model is applied to tapered inductors, the GMD technique will not function so well, due to the difference between each turn width, which is not considered in the GMD calculation. This fact will also introduce some errors in the model.

These limitations are theoretically known, however, in the next chapter, they will be studied in more detail.

4

Model Validation - Results and Discussion

In this chapter the validation of the model will be done through comparisons against ASITIC, an electromagnetic simulator which is widely used by the RF community for inductor simulations [22], and EM simulation with ADS Momentum [21]. Simulations were made for different topologies in 0.13-μm and 0.35-μm CMOS technologies.

Firstly, comparisons were made for the inductance calculation, for square, hexagonal and octagonal topologies, and results are compared to ASITIC. Afterwards, comparisons for inductance, quality factor and SRF are made with ADS Momentum for square, hexagonal and octagonal in a 0.13-μm CMOS technology.

After the comparisons against the 0.13-μm CMOS technology, the model will be tested with the 0.35-μm CMOS technology but only for octagonal layouts, since this topology is the one that presents the higher quality factor values [18]. For this technology a statistical study will be presented.

In order to validate the model for tapered inductors, the model will be compared against square inductors in a 0.13-μm CMOS technology with comparisons against ASITIC and EM simulations. After the comparisons against square inductors, a more detailed study about the improvements and performance of tapered inductors will be done using an octagonal topology in a 0.35-μm CMOS technology.

4.1 Inductance Validation Against ASITIC

Inductance is one of the most important performance parameter in integrated inductors, so it was the first parameter to validate. In this section we present the results obtained

with the proposed model for the validation of the inductance calculation. Results for square, hexagonal and octagonal inductors with non-variable width are presented. The obtained values were checked against results obtained with the field solver ASITIC.

Two working examples, considering areas of 340 $\times$ 340 μm^2 and 290 $\times$ 290 μm^2, are presented in a 0.13 μm CMOS technology. The inductors simulated are summarized in Tables 4.1 and 4.2, the metal width, w is set to 10 μm and the spacing between turns, s, to 5 μm. To reduce the losses the inductors were simulated in metal 8, which has a thickness, t, of 2 μm. The relative error between the value obtained by the model , L_s, and the value given by ASITIC, L_{ast}, is defined as $\varepsilon = 100 \cdot (L_{ast} - L_s)/L_{ast}$.

Sides	n turns	L_s (nH)	L_{ast} (nH)	ε (%)
4	1	1.08	1.08	0.31
4	2	3.27	3.29	0.72
4	3	5.99	6.07	1.21
4	4	8.83	9.06	2.52
4	5	11.71	12.0	2.67
6	1	0.75	0.74	1.35
6	2	2.22	2.19	1.28
6	3	3.97	3.93	0.99
6	4	5.73	5.70	0.60
6	5	7.15	7.29	1.92
8	1	0.77	0.78	1.67
8	2	2.35	2.34	0.51
8	3	4.38	4.24	3.40
8	4	6.32	6.21	1.77
8	5	7.92	8.07	1.94

Table 4.1: L_s value comparison. The inductors have an area of 340 $\times$ 340 um^2.

For square inductors we have typical errors of 2-3%. On the contrary of what was stated by other authors [18], it was possible to design hexagonal and octagonal inductors, with errors typically smaller than 2-3%. For smaller inductors the error is slightly higher and the reason, as explained in [22], is that the inductance has large relative errors for low inductance values.

Sides	n turns	L_s (nH)	L_{ast} (nH)	ε (%)
4	1	0.88	0.88	0.51
4	2	2.62	2.64	0.67
4	3	4.71	4.75	0.87
4	4	6.76	6.92	2.24
4	5	8.62	8.94	3.58
6	1	0.60	0.59	1.69
6	2	1.74	1.72	1.16
6	3	3.04	3.00	1.27
6	4	4.24	4.22	0.57
6	5	5.05	5.20	2.92
8	1	0.62	0.63	1.90
8	2	1.86	1.84	0.81
8	3	3.34	3.26	2.58
8	4	4.79	4.64	3.23
8	5	5.80	5.84	0.77

Table 4.2: L_s value comparison. The inductors have an area of 290 $\times$ 290 um^2.

4.2 Model Validation Against ADS Momentum and ASITIC for a 0.13-μm CMOS Technology

After the validation of inductance model against ASITIC, the model was validated in a 0.13-μm CMOS Technology against EM simulation with ADS Momentum. Fig 4.1, Fig. 4.2 and Fig. 4.3 show the inductors layout simulated in ADS Momentum. It should be mentioned that the simulated layouts were exported from ASITIC and then integrated in ADS Momentum. However, for hexagonal and octagonal layouts, the via connecting metal 8 and metal 7, as well as the underpass metal 7 were added, since ASITIC does not draw or simulate the via and the underpass metal for these layouts.

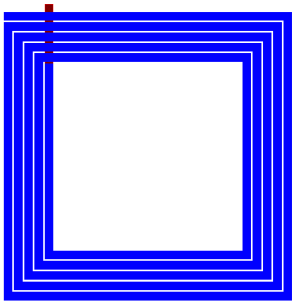


Figure 4.1: Square topology used for simulation in a 0.13-μm CMOS Technology.

Table 4.3 summarize the results for the quality factor and SRF (in GHz) values for the inductors already presented in Table 4.1, and the errors obtained for each parameter. The Q value is measured at the frequency where the inductance value has increased 5% from

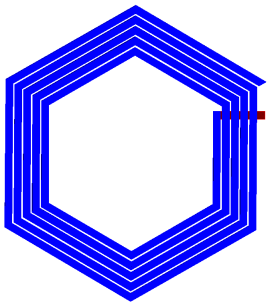


Figure 4.2: Hexagonal topology used for simulation in a 0.13-μm CMOS Technology.

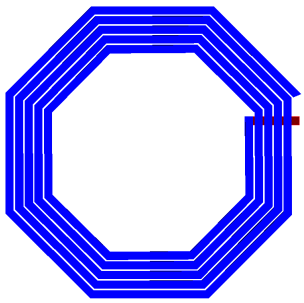


Figure 4.3: Octagonal topology used for simulation in a 0.13-μm CMOS Technology.

the DC inductance value[1]. As previously mentioned, for hexagonal and octagonal layouts, ASITIC does not consider the underpass metal, therefore neglecting the capacitance C_o, and inducing higher errors in SRF.

In Table 4.3, there are two types of errors: the error of the ASITIC values with respect to the EM values and the error of the performance values calculated by the model with respect to the values obtained by EM simulation. The objective is to observe the accuracy of the model with respect to the EM simulations and compared it also to the accuracy of ASITIC. In both cases, the error is calculated as follows, $\varepsilon = 100 \cdot (L_{EM} - L_{\text{Model or ASITIC}})/L_{EM}$. The fitting factor, x, used on the capacitances was 0.35. The model presents quality factor errors of an average value of 4% with respect to EM simulations, which are smaller than the 11% in ASITIC. The SRF value has an average error value of 5% and ASITIC presents an average error of 25%. when compared with EM simulations.

Fig. 4.4, Fig. 4.5 and Fig. 4.6 present comparisons between the model and EM simulations for inductance and quality factor curves for square, hexagonal and octagonal inductors with 3 and 4 turns.

[1]The inductor Q was measured at that frequency basically because that would be the maximum frequency at which the inductor could be used.

Sides	n	SRF_M	SRF_{ADS}	SRF_{AST}	ε_M (%)	ε_{AST} (%)	Q_M	Q_{ADS}	Q_{AST}	ε_M (%)	ε_{AST} (%)
4	2	9.70	10.50	8.32	**7.62**	**20.73**	2.29	2.38	2.50	**3.70**	**5.04**
4	3	7.30	7.30	5.39	**0.00**	**26.21**	2.37	2.37	2.53	**0.00**	**6.75**
4	4	5.60	5.65	4.03	**0.88**	**28.65**	2.05	1.94	2.43	**5.88**	**25.26**
4	5	4.50	5.25	3.27	**14.29**	**37.71**	2.09	2.09	2.56	**0.10**	**22.49**
6	2	11.85	12.70	10.48	**6.69**	**17.48**	2.77	2.81	2.95	**1.42**	**4.98**
6	3	9.00	8.70	6.77	**3.45**	**22.22**	2.92	2.82	2.96	**3.55**	**4.96**
6	4	6.80	6.85	5.09	**0.73**	**25.69**	2.73	2.52	2.63	**8.33**	**4.37**
6	5	5.45	5.70	4.13	**4.39**	**27.47**	2.53	2.15	2.37	**17.67**	**10.23**
8	2	10.80	12.10	10.02	**10.74**	**17.19**	2.74	2.70	2.40	**1.48**	**3.70**
8	3	8.00	8.30	6.44	**3.61**	**22.46**	2.47	2.38	2.46	**4.00**	**3.58**
8	4	6.00	6.50	4.75	**7.96**	**26.92**	2.69	2.46	2.04	**9.35**	**17.07**
8	5	4.80	5.40	3.87	**11.11**	**28.33**	2.43	2.20	2.28	**10.45**	**3.64**

Table 4.3: SRF in GHz and Q values for the proposed model. ASITIC and EM ADS Momentum simulations in a 0.13-μm CMOS Technology.

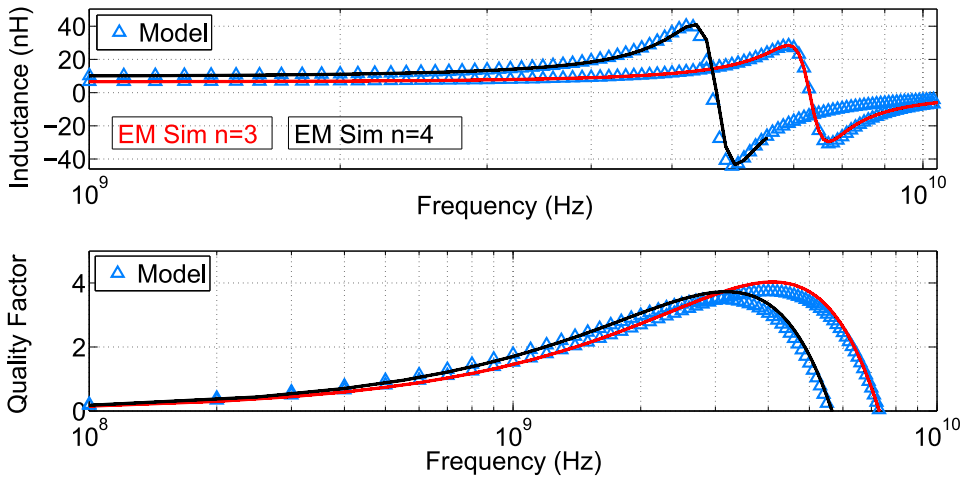


Figure 4.4: EM simulation data (solid line) compared with the model for a 3 and 4 turn square inductor in a 0-13 μm CMOS technology.

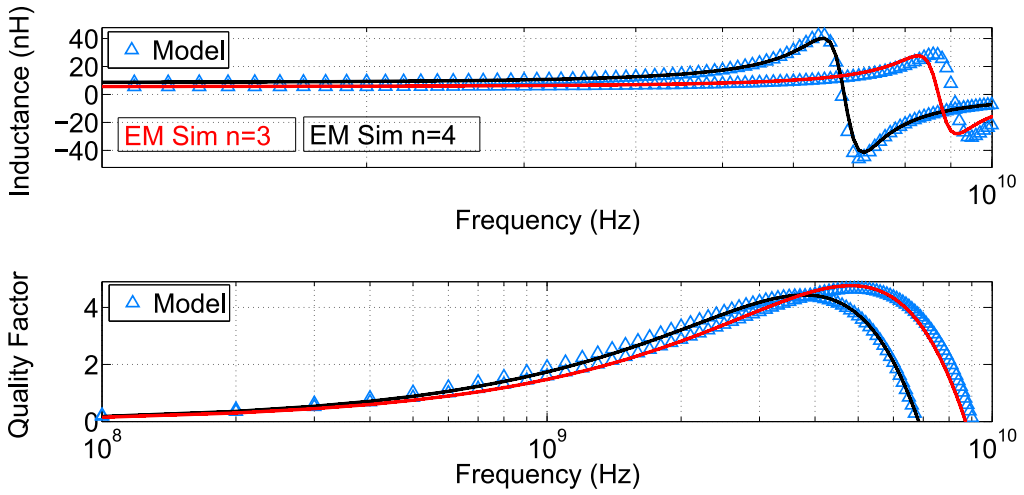


Figure 4.5: EM simulation data (solid line) compared with the model for a 3 and 4 turn hexagonal inductor in a 0-13 μm CMOS technology.

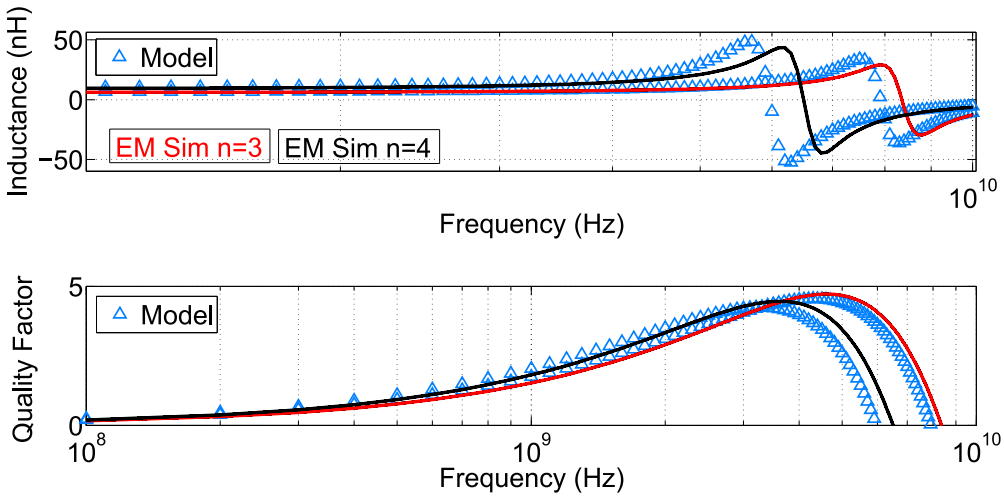


Figure 4.6: EM simulation data (solid line) compared with the model for a 3 and 4 turn octagonal inductor in a 0-13 μm CMOS technology.

4.3 Model Validation Against ADS Momentum for a 0.35-μm CMOS Technology

The model has also been validated for a 0.35-μm CMOS technology. The topology used for this study can be seen in Fig 4.7.

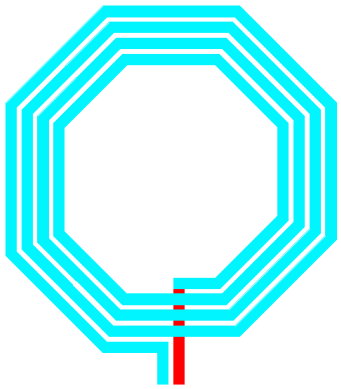


Figure 4.7: Octagonal topology used for simulation in a 0.35-μm CMOS Technology.

Comparisons were made for an octagonal topology, against a high number of inductors, whose geometric parameters were generated using the latin hypercube sampling (LHS) strategy in order to perform a statistical study of the model performance [91]. Table 4.4 shows the ranges for the different variables. It is important to mention that the spacing between metals, s, was the only geometric parameter which was kept constant at 2.5 μm over the entire LHS process, which corresponds to the minimum spacing allowed by the technology. A total of 1000 inductors were obtained by this method and simulated both with ADS Momentum and our model.

Parameter	Minimum	Maximum
n	1	10
D_{in} (μm)	10	250
w (μm)	5	25

Table 4.4: Geometrical variable ranges for the inductors parameters generated with LHS.

The comparative study made for the 1000 inductors showed that the model does not fit well over all the design space. For example, for small inner diameters, the Eddy currents tend to increase, and the model does not take into account Eddy currents, increasing the model errors. Also, with an bigger w, the parasitic capacitances and fringing capacities tend to increase and induce higher errors in the model. Therefore, only those inductors whose geometric parameters fit in the ranges included in Table 4.5, are considered for the further analysis.

Parameter	Minimum	Maximum
n	2	7
D_{in} (μm)	100	250
w (μm)	5	10
SRF (GHz)	4	20

Table 4.5: Restrictions on the inductors parameters for comparison with the model.

These geometric parameter restrictions are in agreement with the approximations made in the model. Besides the D_{in} limitations due to Eddy currents, the maximum number of turns is limited to 7, although it could be increased by changing the equations of the model. On the other hand, approximations on the capacitances calculation will make it hard for the model to fit EM simulations for values above 20 GHz. From the 1000 inductors generated, only 327 fulfil the conditions mentioned in Table 4.5. This conditions also respect the design rules, shown in Eq. 4.1, aiming to reduce the parasitic phenomena due to high frequency effects, such as the proximity effect.

$$0.2 < D_{in}/D_{out} < 0.8 \text{ and } D_{in} > 5w \tag{4.1}$$

The results of the statistical study for the 327 inductors are shown in Fig. 4.8, Fig. 4.9 and Fig. 4.10, for the inductance at 100 kHz[2], quality factor (peak value) and SRF, respectively. For the inductance, the average error values is 4%. The quality factor at the peak value and the SRF calculation both have an average error of 2%. The fitting factor, x, used on the capacitances was 0.25, and another fitting factor of 1.25 was used on the series resistance, R_s.

It is possible to observe that the most difficult parameter to model is the SRF, which depends mostly on the parasitic capacitances. The inductance value is well defined also

[2]This value was used in order to validate the inductance at low frequencies.

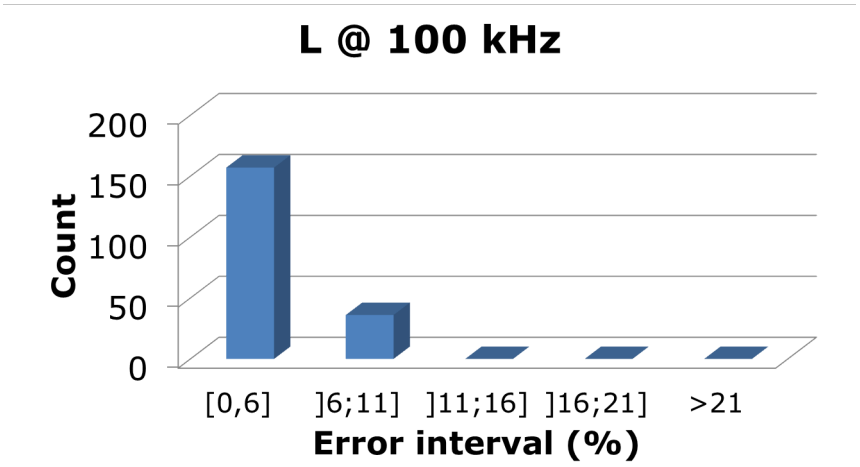


Figure 4.8: Inductor count over the different error intervals for the inductance value at 100 kHz.

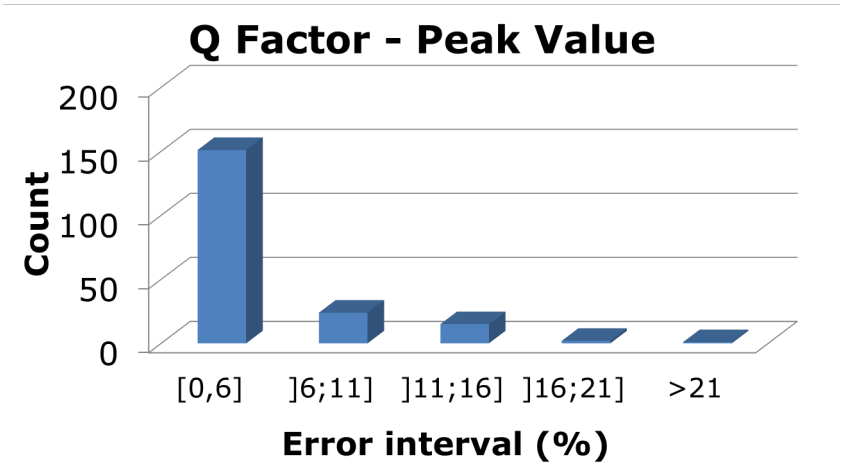


Figure 4.9: Inductor count over the different error intervals for the quality factor, in its peak value.

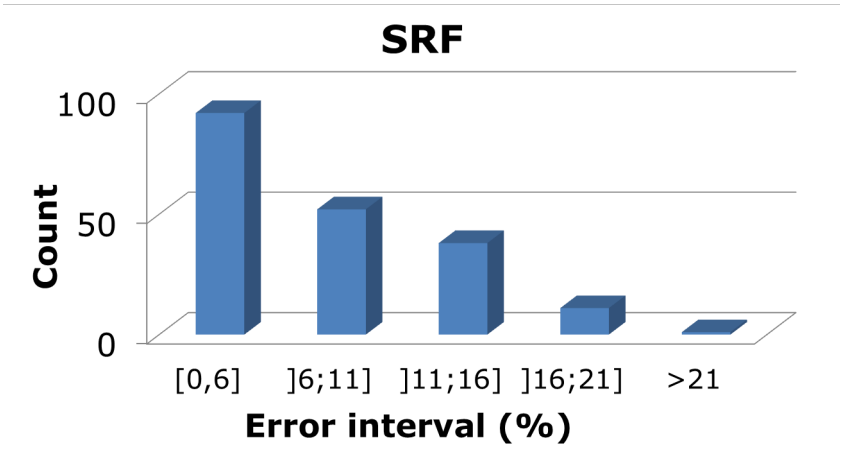


Figure 4.10: Inductor count over the different error intervals for the SRF.

as the quality factor at its peak value.

4.4 Tapered Width Inductors

In this section results for octagonal and square tapered inductors are presented. The objective of this section is to study the improvements on integrated inductor performances by the usage of different turn widths. Firstly, square tapered inductors are compared against ASITIC and EM simulation in a 0.13-μm CMOS technology. Afterwards, octagonal tapered inductors performances are compared against EM simulation in a 0.35-μm CMOS technology.

4.4.1 Model Validation Against ASITIC and ADS Momentum in a 0.13-μm CMOS Technology for Square Tapered Inductors

In this section, the inductance calculation was validated against ASITIC in a first stage (because ASITIC simulation is much quicker than EM simulation), in order to prove that the inductance calculation method could be used with tapered inductors in a 0.13-μm CMOS technology. Square inductors simulated in this section increase width from segment to segment. This type of layout is impossible to obtain in other different topologies such as octagonal, because the inner angle of the octagonal would change.

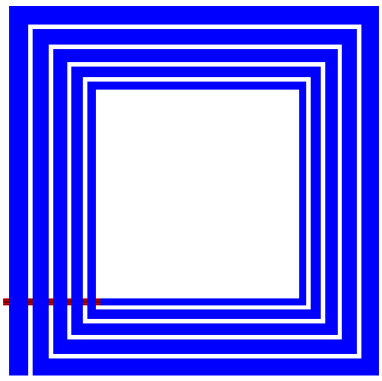


Figure 4.11: Square tapered integrated inductor.

The expression used to increase the width of the inductor is given in Eq. 4.2, which is also used by ASITIC,

$$w_i^2 = w_0 + (w_1 - w_0) \cdot \frac{i}{4 \cdot n} \tag{4.2}$$

where w_0 is the last segment of the last turn, w_1 is the first segment of the first turn, i is the number of the segment and n is the number of turns. The results obtained are shown in Table 4.6.

The errors obtained are similar to the errors obtained in equal width inductors, with average errors of 2%. So, it is possible to conclude that the inductance calculation method

n turns	D_{out}	w_i	w_f	s	$L_s\ (nH)$	$L_{ast}\ (nH)$	ε (%)
2	300	5	10	2.5	3.00	3.00	0.00
3	300	5	10	2.5	5.74	5.68	1.05
4	300	5	10	2.5	8.78	8.68	1.14
5	300	5	10	2.5	11.87	11.79	0.67
2	350	5	15	3.5	3.33	3.33	0.00
3	350	5	15	3.5	6.30	6.20	1.59
4	350	5	15	3.5	9.52	9.27	2.63
5	350	5	15	3.5	12.67	12.32	2.76
2	400	5	15	4.5	3.96	3.98	0.51
3	400	5	15	4.5	7.50	7.43	0.93
4	400	5	15	4.5	11.37	11.23	1.23
5	400	5	15	4.5	15.25	15.10	0.98
2	450	10	35	7	3.32	3.38	1.69
3	450	10	35	7	5.77	5.67	1.76
4	450	10	35	7	7.76	7.57	2.51
5	450	10	35	7	8.88	8.77	1.02

Table 4.6: L_s value comparison for a tapered width square layout. The physical parameters are given in um

is also valid for tapered inductors.

Afterwards, two working examples were considered in order to validate the model against EM simulations. In the first working example, the inductors have an area of 350×350 μm^2, with the first segment of the inner turn having a width, w_i=5 μm, an the last segment of the last turn having a width, w_0=10 μm and a spacing between metals, s=2.5 μm. The results for the inductance calculation are shown in Table 4.7 and the results for the SRF and the quality factor are shown in Table 4.8. Again, the Q value is measured at the frequency where the inductance increased 5% from DC inductance.

Sides	n	L_M	L_{ast}	L_{ADS}	ε_M (%)	ε_{AST} (%)
4	2	3.76	3.70	3.65	**1.62**	**1.35**
4	3	7.32	7.04	6.90	**3.98**	**1.99**
4	4	11.42	10.84	10.52	**5.35**	**2.95**
4	5	15.77	14.86	14.26	**6.12**	**4.04**

Table 4.7: Square tapered L_s results for the proposed model comparing with ASITIC and EM ADS Momentum simulations.

In Table 4.8 it is possible to observe the results for the quality factor and SRF (in GHz) values, and the errors obtained for each parameter. As previously mentioned, ASITIC does not consider the underpass metal, therefore neglecting the capacitance C_o, inducing higher errors in SRF. In Fig. 4.12 it is possible to observe the comparison curves between the model and EM simulation.

Sides	n	SRF_M	SRF_{ADS}	SRF_{AST}	ε_M (%)	ε_{AST} (%)	Q_M	Q_{ADS}	Q_{AST}	ε_M (%)	ε_{AST} (%)
4	2	9.30	10.40	9.75	**10.28**	**6.25**	2.80	3.30	4.33	**15.15**	**31.21**
4	3	7.25	7.20	6.20	**0.69**	**13.89**	3.10	3.11	4.65	**0.32**	**49.52**
4	4	5.60	5.70	4.55	**1.75**	**20.15**	3.00	2.99	4.33	**0.33**	**44.82**
4	5	4.45	4.80	3.62	**7.29**	**24.58**	2.85	2.89	4.01	**1.52**	**38.75**

Table 4.8: Square tapered SRF and Q values for the proposed model. ASITIC and EM ADS Momentum simulations.

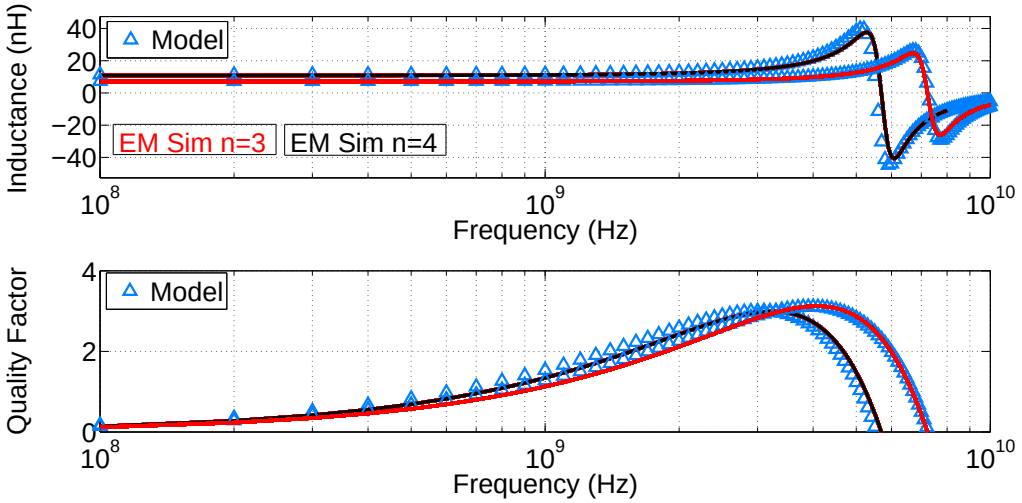


Figure 4.12: EM simulation data (solid line) compared with the model for a 3 and 4 turn square tapered inductor.

The second example is for inductors with an area of 300×300 μm^2, with the first segment of the inner turn having a width, w_i=5 μm, an the last segment of the last turn having a width, w_0=15 μm and a spacing between metals, s=4 μm. The results for the inductance calculation are presented in Table 4.9 and the results for the SRF and quality factor are presented in Table 4.10.

Sides	n	L_M	L_{ast}	L_{ADS}	ε_M (%)	ε_{AST} (%)
4	2	2.68	2.66	2.64	**1.52**	**0.68**
4	3	4.97	4.71	4.80	**3.58**	**1.83**
4	4	7.32	6.79	6.95	**5.32**	**2.30**
4	5	9.48	8.88	8.87	**6.88**	**0.14**

Table 4.9: Square tapered L_s results for the proposed model. ASITIC and EM ADS Momentum simulations.

It is possible to conclude that the model works well for square tapered inductors, with average inductance errors being less than 2 %, the SRF average error is 10 % and the quality factor average error is 6 %. The SRF calculation and the quality factor have higher errors than equal width inductors. This fact may be explained because the capacitances fitting factors do not work so well due to the changes on the segment width. This will

Sides	n	SRF_M	SRF_{ADS}	SRF_{AST}	ε_M (%)	ε_{AST} (%)	Q_M	Q_{ADS}	Q_{AST}	ε_M (%)	ε_{AST} (%)
4	2	14.50	13.30	12.95	**9.02**	**2.63**	2.49	2.58	2.76	**3.72**	**6.82**
4	3	10.90	9.50	8.01	**14.74**	**15.65**	2.90	2.82	3.09	**2.95**	**9.59**
4	4	8.50	8.90	6.10	**4.49**	**31.46**	2.72	2.49	2.76	**9.24**	**10.84**
4	5	7.90	7.90	5.06	**11.39**	**35.95**	2.62	2.41	2.59	**8.50**	**7.34**

Table 4.10: Square tapered SRF and Q values for the proposed model and the comparisons with ASITIC and EM ADS Momentum simulations.

make quite difficult to find the perfect fitting factor.

4.4.2 Performance Study of Octagonal Tapered Inductors in a 0.35-μm CMOS Technology

In order to properly analyse the performance of tapered inductors, the range of the turn width, w, used in section 4.3 had to be increased to 20 μm, therefore, new fitting factors had to be used, changing therefore the model. The fitting factor, x, used on the capacitances was 0.4, and the R_s fitting factor was 1.3. Also it should be mentioned that, according to the statistical analysis, there are expected larger errors since the model fits a larger region. The model was only compared with ADS Momentum in this section because ASITIC does not simulate octagonal tapered inductors. In Fig 4.13 is possible to observe the inductor layout as simulated in ADS Momentum.

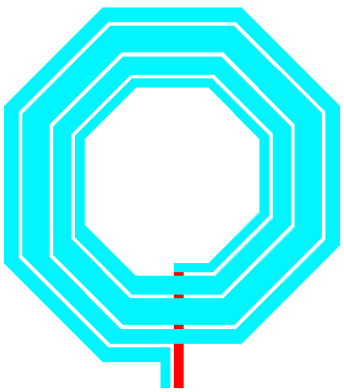


Figure 4.13: Octagonal tapered topology used for simulation in a 0.35-μm CMOS Technology.

Simulations were made for inductors from two to six turns, varying the width of each turn and the D_{in}. The turn width variations were made from 5 μm to 20 μm.

For two turn inductors, several variations on the layout are presented in Table 4.11, where D_{in}, the inner diameter, and w_1 and w_2 are the width of the first and second turn respectively.

From the EM simulation, it can be seen that there is a width were the quality factor is higher, and then starts to decrease as the widths of each turn start reaching equality. However, the model does not have the same behaviour. This happens not only for the

Id	D_{in}	w_1	w_2	Area
0	245	5	20	300
1	239	8	20	300
2	233	11	20	300
3	227	14	20	300
4	221	17	20	300
5	215	20	20	300

Table 4.11: Physical parameters of the simulated octagonal inductors with two turns.

Id	L_M	L_{ADS}	ε_M (%)	Q_M	Q_{ADS}	ε_M (%)	SRF_M	SRF_{ADS}	ε_M (%)
0	2.12	2.35	**9.87**	7.35	9.50	**22.63**	11.00	14.60	**24.66**
1	2.00	2.19	**8.68**	8.53	10.57	**19.32**	10.90	14.40	**24.31**
2	1.91	2.07	**7.68**	9.34	10.98	**14.90**	10.90	14.40	**24.31**
3	1.84	1.97	**6.41**	9.90	11.07	**10.57**	10.80	14.50	**25.52**
4	1.78	1.87	**4.65**	10.28	11.05	**6.97**	10.80	14.50	**25.52**
5	1.73	1.78	**2.81**	10.56	10.94	**3.47**	10.70	15.50	**30.97**

Table 4.12: Two turn octagonal tapered SRF and Q values for the proposed model and the comparisons with EM ADS Momentum simulations.

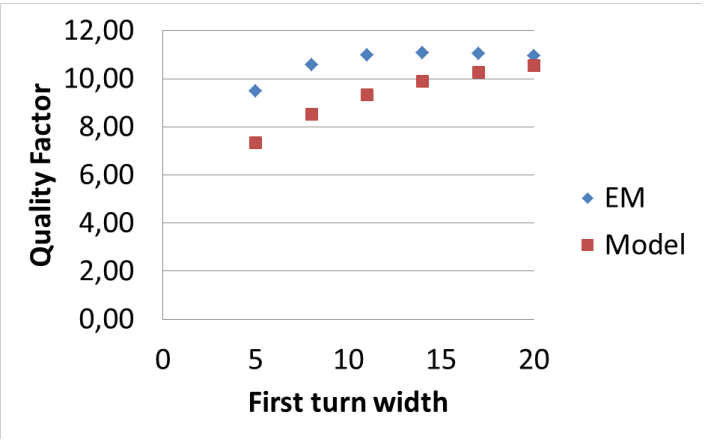


Figure 4.14: Two turn inductor values over the different physical parameters for the quality factor peak value.

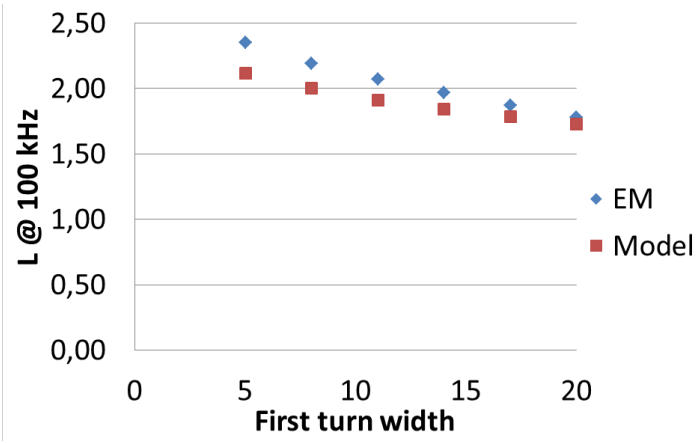


Figure 4.15: Two turn inductor values over the different physical parameters for the inductance value at 100 kHz.

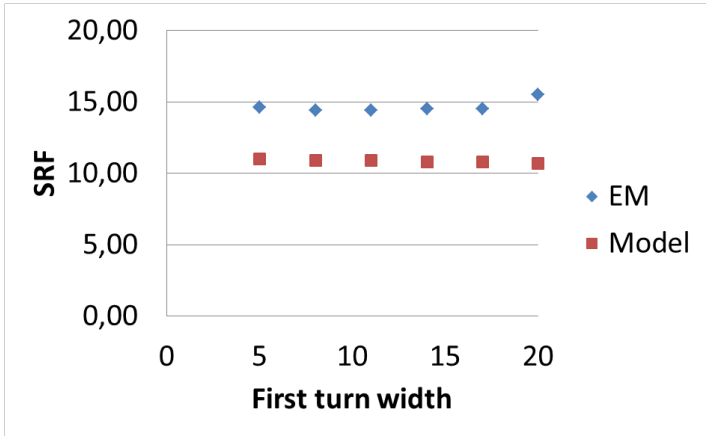


Figure 4.16: Two turn inductor values over the different physical parameters for the SRF value.

Id	D_{in}	w_1	w_2	w_3	Area
0	215	5	12.5	20	300
1	206	8	14	20	300
2	197	11	15.5	20	300
3	188	14	17	20	300
4	179	17	18.5	20	300
5	170	20	20	20	300

Table 4.13: Physical parameters of the simulated octagonal inductors with three turns.

Id	L_M	L_{ADS}	ε_M (%)	Q_M	Q_{ADS}	ε_M (%)	SRF_M	SRF_{ADS}	ε_M (%)
0	4.37	4.33	**0.88**	8.04	8.41	**4.44**	8.90	9.60	**7.29**
1	3.86	4.00	**3.45**	8.59	9.07	**5.28**	9.20	9.50	**3.16**
2	3.60	3.71	**2.86**	9.05	9.33	**3.02**	9.40	9.60	**2.08**
3	3.43	3.46	**0.84**	9.42	9.42	**0.04**	9.40	9.65	**2.59**
4	3.30	3.23	**2.23**	9.70	9.39	**3.36**	9.40	9.80	**4.08**
5	3.20	3.00	**6.63**	9.93	9.22	**7.65**	9.40	11.30	**16.81**

Table 4.14: Three turn octagonal tapered SRF and Q values for the proposed model and the comparisons with EM ADS Momentum simulations.

two turn inductors, but also for all n-turn inductors. The model presents a 6% average error in the inductance calculation, a 12% in the quality factor calculation, at its peak value and 25% at the SRF calculation.

In Table 4.13 the physical parameters of the three turn inductors simulated are presented.

For this case, the model presents a 3% average error in the inductance calculation, a 4% in the quality factor calculation, at its peak value, and 6% at the SRF calculation. It is possible to state that the model is much more accurate for inductors with three turn than it is with two turns. This may be due to the fitting parameters or due to the lumped element analytical equations that fit better this range of frequencies, as it can been seen, all the SRF values for three turn inductors are in the 9 GHz range, which are lower than for two turn inductors.

In Table 4.15 the physical parameters of the four turns inductors simulated are presented.

For the case of four turn inductors, the model presents a 5% average error in the inductance calculation, a 5% in the quality factor calculation, at its peak value and 7% at the SRF calculation. It starts to be observable in Fig. 4.20. that the quality factor peak values of the EM simulations and the model are going in opposite directions. This fact may also be due to the lumped element analytical equations. This physical equations were developed for perfect rectangular segments. For tapered inductors, specially in hexagonal and octagonal topologies, each segment is not a perfect rectangle, so the length of each segment is approximated by an average between the outer trace and the inner

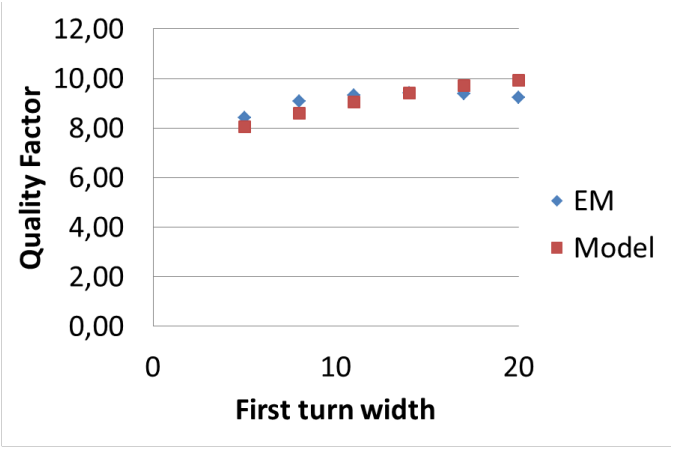


Figure 4.17: Three turn inductor errors over the different physical parameters for the quality factor peak value.

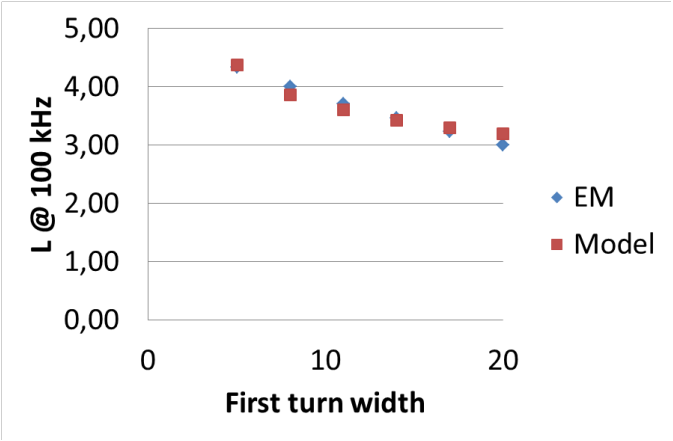


Figure 4.18: Three turn inductor errors over the different physical parameters for the inductance value at 100 kHz.

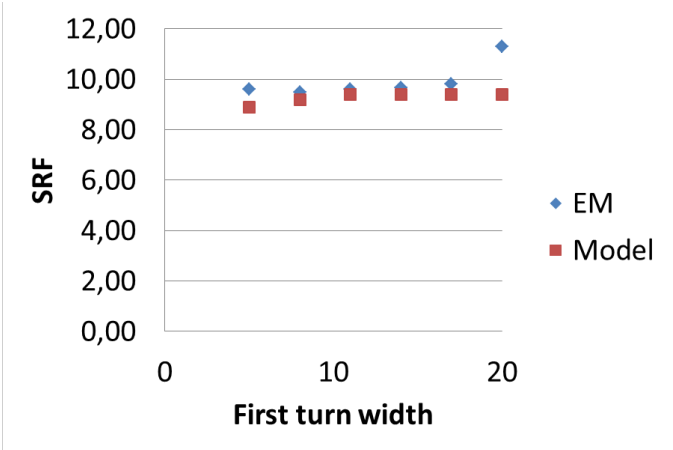


Figure 4.19: Three turn inductor errors over the different physical parameters for the SRF value.

Id	D_{in}	w_1	w_2	w_3	w_4	Area
0	185	5	10	15	20	300
1	173	8	12	16	20	300
2	161	11	14	17	20	300
3	149	14	16	18	20	300
4	137	17	18	19	20	300
5	125	20	20	20	20	300

Table 4.15: Physical parameters of the simulated octagonal inductors with four turns.

Id	L_M	L_{ADS}	ε_M (%)	Q_M	Q_{ADS}	ε_M (%)	SRF_M	SRF_{ADS}	ε_M (%)
0	7.03	6.47	**8.72**	8.19	7.87	**4.07**	7.00	7.20	**2.78**
1	5.70	5.88	**2.99**	8.23	8.34	**1.38**	7.50	7.20	**4.17**
2	5.21	5.36	**2.80**	8.49	8.51	**0.20**	7.90	7.30	**8.22**
3	4.92	4.88	**0.84**	8.76	8.48	**3.30**	8.00	7.50	**6.67**
4	4.72	4.46	**5.83**	9.00	8.37	**7.49**	8.00	7.80	**2.56**
5	4.56	4.07	**12.15**	9.20	8.13	**13.20**	8.00	9.70	**17.53**

Table 4.16: Four turn octagonal tapered SRF and Q values for the proposed model and the comparisons with EM ADS Momentum simulations.

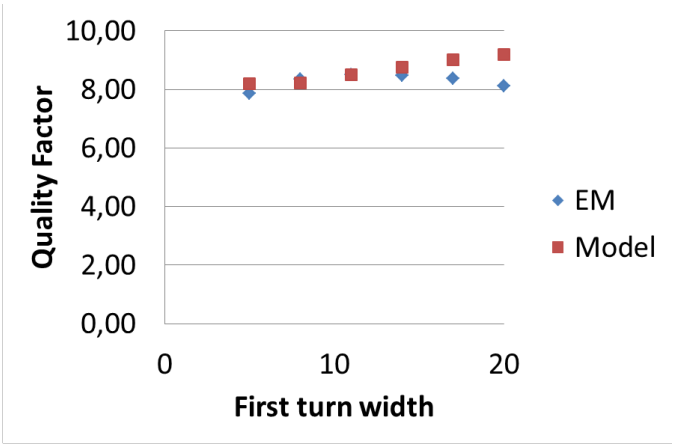


Figure 4.20: Four turn inductor errors over the different physical parameters for the quality factor peak value.

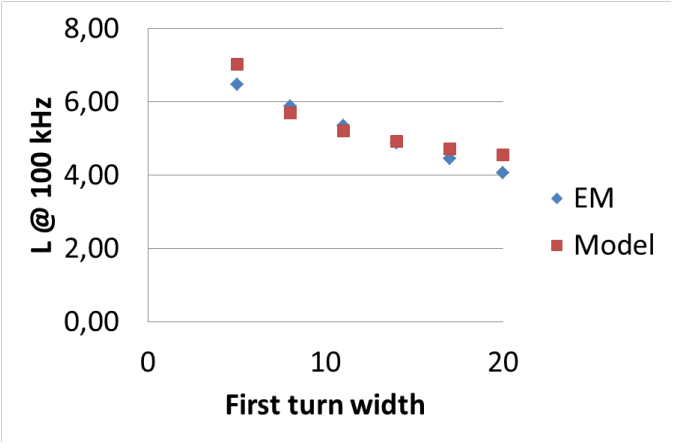


Figure 4.21: Four turn inductor errors over the different physical parameters for the inductance value at 100 kHz.

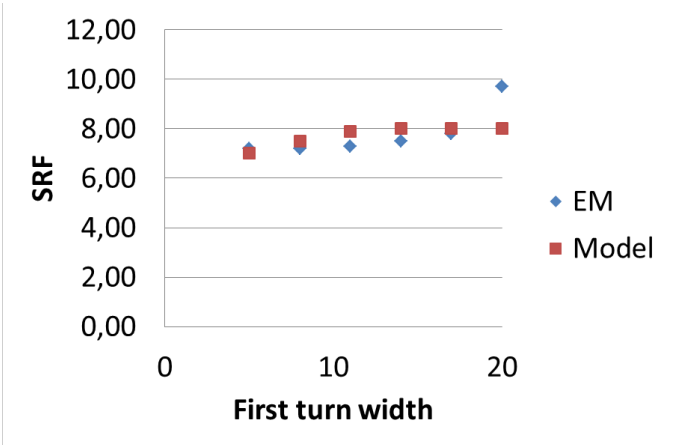


Figure 4.22: Four turn inductor errors over the different physical parameters for the SRF value.

Id	D_{in}	w_1	w_2	w_3	w_4	w_5	Area
0	157	5	8.5	12	16	20	300
1	140	8	11	14	17	20	300
2	127	11	13	15	17.5	20	300
3	110	14	15.5	17	18.5	20	300
4	92	17	18	19	20	20	300
5	80	20	20	20	20	20	300

Table 4.17: Physical parameters of the simulated octagonal inductors with five turns.

Id	L_M	L_{ADS}	ε_M (%)	Q_M	Q_{ADS}	ε_M (%)	SRF_M	SRF_{ADS}	ε_M (%)
0	10.10	8.72	**15.79**	8.38	7.44	**12.69**	5.80	5.70	**1.75**
1	7.33	7.66	**4.35**	8.06	7.84	**2.77**	6.60	6.00	**10.00**
2	6.67	6.90	**3.38**	8.18	7.94	**3.06**	6.80	6.00	**13.33**
3	6.18	6.08	**1.66**	8.42	7.80	**7.98**	7.00	6.40	**9.37**
4	5.83	5.31	**9.85**	8.70	7.49	**16.18**	7.00	7.20	**2.78**
5	5.73	4.78	**19.89**	8.86	7.24	**22.47**	7.10	9.00	**21.11**

Table 4.18: Five turn octagonal tapered SRF and Q values for the proposed model and the comparisons with EM ADS Momentum simulations.

trace, for each segment. This fact may induce errors in the calculations of capacitances and resistances which also affects inductance. Also, for tapered inductors, this error may be larger because each segment has a different width in each side (lateral side) and this length is approximated. With the fitting factors it is possible to reach a reasonable error value, however this fitting factor would not be suitable for the entire frequency range.

In Table 4.17 the physical parameters of the five turn inductors simulated are presented.

For the case of five turn inductors, the model presents a 9% average error in the inductance calculation, a 10% in the quality factor calculation, at its peak value, and 9% at the SRF calculation. Once again, it is possible to observe in Fig. 4.23 the opposite direction that the quality factor curve of the EM simulations and the model are taking.

In Table 4.19 the physical parameters of the six turn inductors simulated are presented.

Id	D_{in}	w_1	w_2	w_3	w_4	w_5	w_6	Area
0	125	5	8	11	14	17	20	300
1	105	8	10.5	13	15.5	18	20	300
2	86	11	13	15	17	18.5	20	300
3	74	14	15	16	17	18.5	20	300
4	50	17	17.5	18.5	19.5	20	20	300
5	35	20	20	20	20	20	20	300

Table 4.19: Physical parameters of the simulated octagonal inductors with six turns.

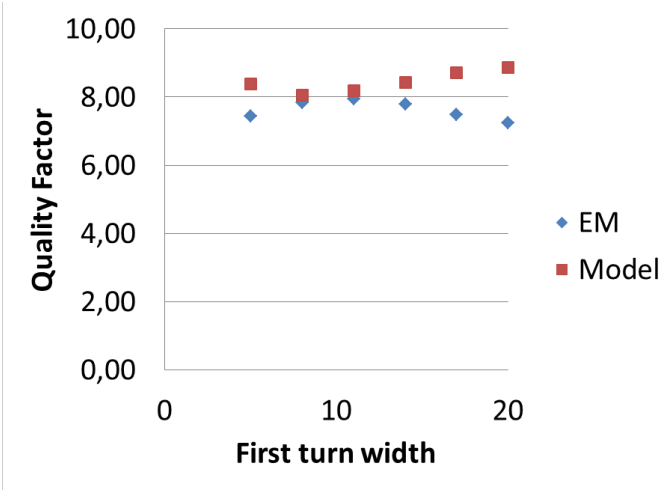


Figure 4.23: Five turn inductor errors over the different physical parameters for the quality factor peak value.

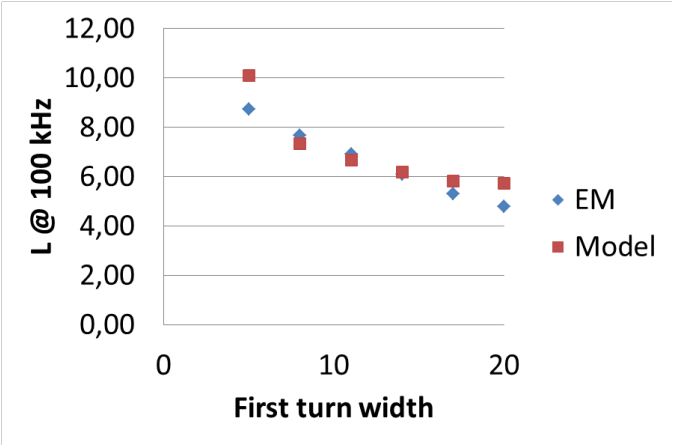


Figure 4.24: Five turn inductor errors over the different physical parameters for the inductance value at 100 kHz.

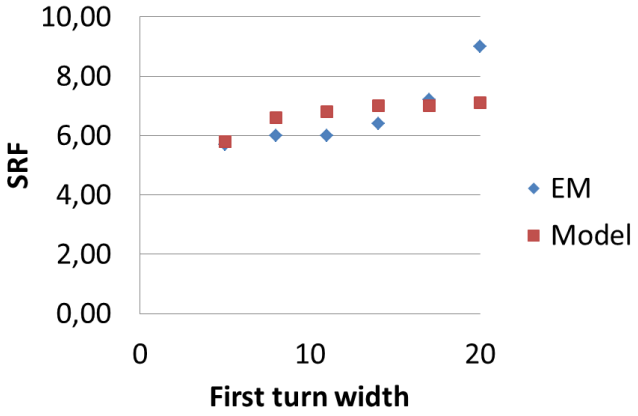


Figure 4.25: Five turn inductor errors over the different physical parameters for the SRF value.

Id	L_M	L_{ADS}	ε_M (%)	Q_M	Q_{ADS}	ε_M (%)	SRF_M	SRF_{ADS}	ε_M (%)
0	12.24	10.62	**15.25**	8.70	7.12	**22.19**	5.00	5.40	**7.41**
1	8.49	9.13	**7.04**	8.09	7.38	**9.62**	5.30	6.40	**17.19**
2	7.53	7.88	**4.54**	8.22	7.35	**11.84**	6.80	5.50	**23.64**
3	7.26	7.07	**2.69**	8.20	7.20	**13.89**	6.80	5.80	**17.24**
4	6.74	5.90	**14.24**	8.69	6.75	**28.74**	6.90	6.50	**6.15**
5	6.60	5.00	**32.00**	8.87	5.18	**71.24**	7.70	6.80	**13.24**

Table 4.20: Six turn octagonal tapered SRF and Q values for the proposed model and the comparisons with EM ADS Momentum simulations.

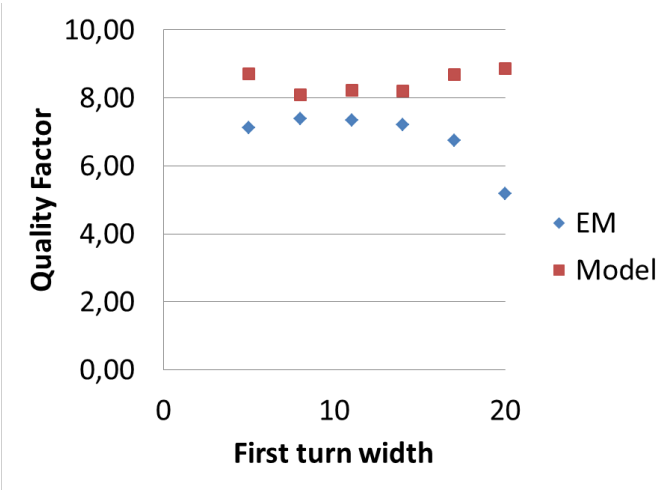


Figure 4.26: Six turn inductor errors over the different physical parameters for the quality factor peak value.

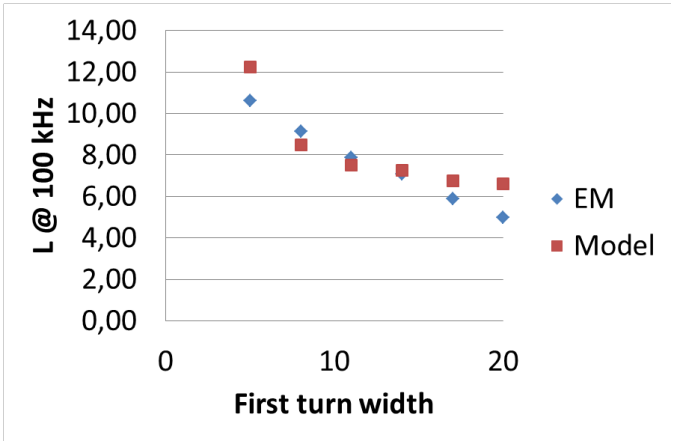


Figure 4.27: Six turn inductor errors over the different physical parameters for the inductance value at 100 kHz.

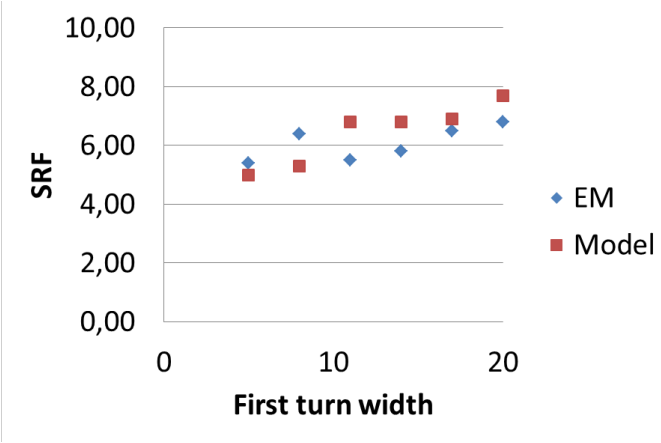


Figure 4.28: Six turn inductor errors over the different physical parameters for the SRF value.

For the case of six turn inductors, the model presents a 12% average error in the inductance calculation, a 26% in the quality factor calculation, at its peak value, and 14% at the SRF calculation. This sudden increase in the error values from five to six turns may be due to the smaller D_{in} value, that reaches the minimum that can be modelled with relative accuracy. It is also important to state that the higher number of segments, the higher is the error of the model.

5

Optimization of Integrated Inductors

This chapter discusses the optimization of octagonal integrated inductors in a 0-35 μm CMOS technology. As previously mentioned the octagonal layout uses less metal than square or hexagonal layouts to achieve a given value of inductance, thus presenting the higher quality factor. This chapter presents two different optimization processes. The first optimization presents a single objective optimization using the selection based differential evolution algorithm (SDBE) and the second optimization is a multi-objective optimization using the non dominating sorting algorithtm-II (NSGA-II). The results of the optimization process will be compared against EM simulations.

5.1 Model Fitting

When the optimization processes was initiated and observing the inductor curves in detail, it was possible to conclude that the fitting factors induced a frequency shift in the quality factor peak value, which became a problem for the optimization process. As it was explained in Chapter 2, an inductor is suitable to be used in the inductance flat-bandwidth zone, which for the higher frequency range, normally corresponds to the frequencies where the quality factor is on the positive slop of the curve. If we observe Fig. 5.1, it is possible to conclude that at 2 GHz, this inductor is no longer suitable to be used at this frequency. However, due to the frequency shift induced by the fitting factors, this inductor is still usable when simulated with the model. The selected inductor has $n = 5$, $w = 7.33$ μm and $D_{in} = 197$ μm.

After analysing the effects of the fitting factors, it was possible to conclude that the shift in frequency was due to the fitting factor in the series resistance, so this fitting factor was removed and the capacitance fitting factors were adapted to achieve a good curve

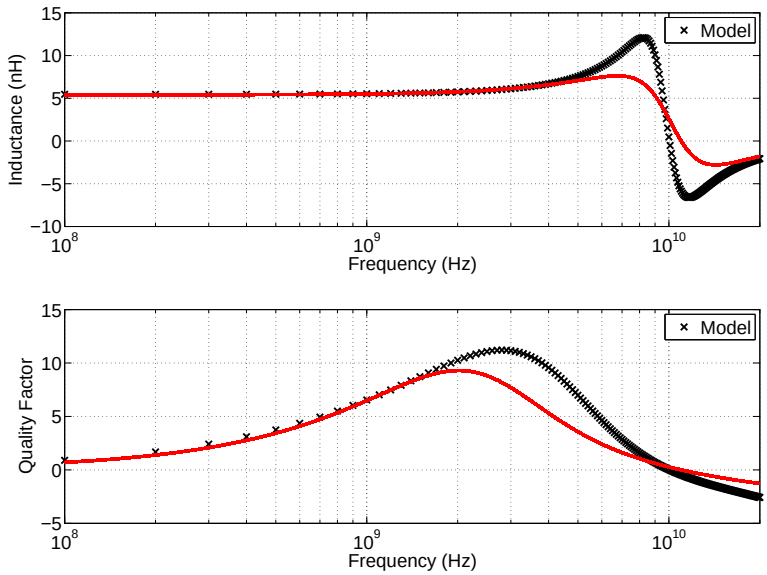


Figure 5.1: EM simulation data (red solid line) compared with the model with the fitting factors for adjusting the SRF value in a 0.35-μm CMOS technology.

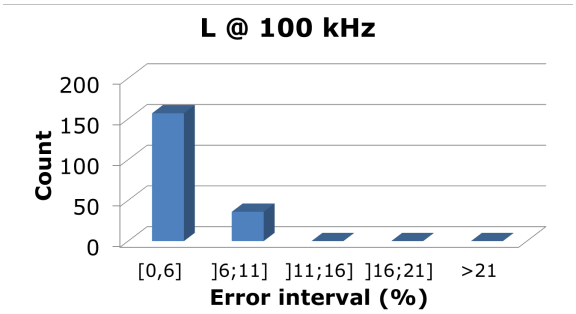


Figure 5.2: Inductor count over the different error intervals for the inductance value at 100 kHz.

fitting. The new fitting factor, x, is 0.5.

So a new statistical study was done for the 194 inductors, and the results are presented in Fig. 5.2, Fig. 5.3 and Fig. 5.4.

It is possible to conclude that the model presents higher errors with these fitting factors, however the quality factor does no longer presents the shift in frequency. The SRF value obtained from the model shows an average error of 25% with respect to the EM simulated value. The SRF value of the model is always bellow the real SRF, this means that the capacitances are being over calculated. It is possible to conclude that the SRF value is the most difficult parameter to approximate, due to its strong dependence on the inductor parasitic capacitances that are not integrated in the model equations [15]. In Fig. 5.5, it is possible to observe the same inductor simulated in Fig. 5.1, but with the new fitting factors.

It is possible to conclude that the fitting factors that are most useful for integrating

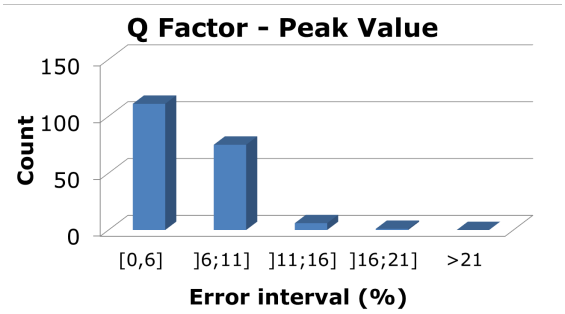


Figure 5.3: Inductor count over the different error intervals for the quality factor, in its peak value.

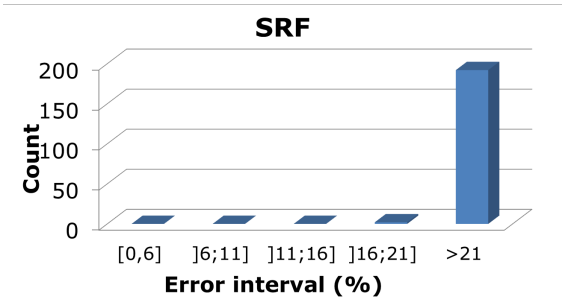


Figure 5.4: Inductor count over the different error intervals for the SRF.

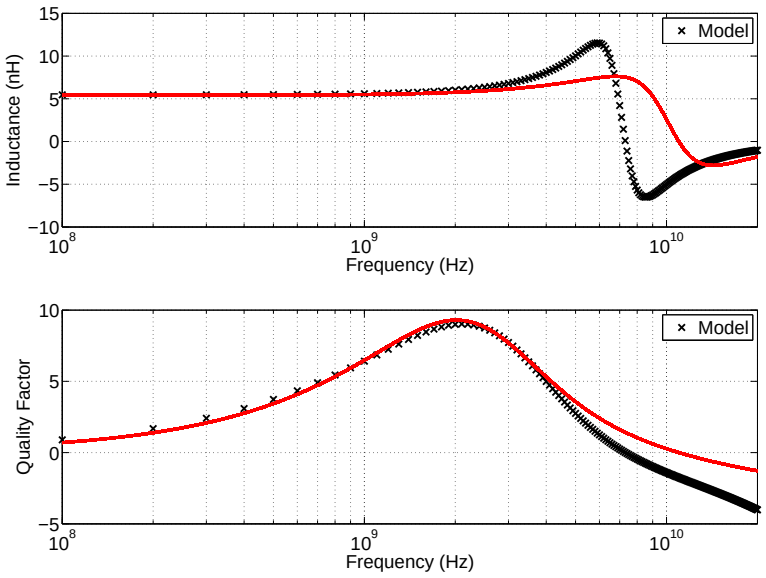


Figure 5.5: EM simulation data (red solid line) compared with the model, for adjusting the quality factor curve in a 0.35-μm CMOS technology.

the model into a optimization process are the ones used for this last statistical analysis, once the quality factor curve is well defined over the entire range of useful frequencies.

5.2 Optimization Process

Both single and multi-objective optimization processes need objectives and constraints. The objectives are values that the optimization algorithm tries to maximize or minimize, and the constraints are used as boundaries to which the given solution must comply. As the name indicates, in single-objective optimization processes, only one objective is maximized or minimized. On the other hand, multi-objective optimization processes may have several objectives. In the case of the single objective, if one desires to include several objectives into one optimization process, it is possible to built a objective function, where the different variables are given weights. Also in the single-objective optimization, there is a violation function which is related with the constraints used. The one used in this work, for single-objective simulation is presented in Eq. 5.1. The work frequency is 2.4 GHz for both optimization processes. In the multi-objective optimization the constraints used were the same but there is no need to use a violation function.

$$\begin{aligned} Violation = min(0.05 - abs((L_{M@2.4GHz} - L_{desired})/L_{desired}), 0)+ \\ min(0.1 - abs((L_{DC} - L_{M@2.4GHz})/L_{M@2.4GHz}), 0)+ \\ min((Q_{M@2.5GHz} - Q_{M@2.4GHz}), 0) \end{aligned} \quad (5.1)$$

Through the violation equation it is possible to observe that the constraints that are applied are:

- The inductance value is limited to only 5% error from the inductance desired at 2.4 GHz,
- The inductance curve has to be in the plain bandwidth zone, which means that the inductance value can only vary 10% from the DC value,
- The quality factor has to be before the peak value, which means that the quality factor has to be in the positive slope region of the quality factor curve.

5.3 Single Objective Optimization - SBDE

Selection-based differential evolution evolution (SBDE) is a method that optimizes a problem by iteratively trying to improve a candidate solution with regard to a given measure of quality. Such methods are commonly known as metaheuristics as they make few or no assumptions about the problem being optimized and can search very large spaces of candidate solutions. SBDE optimizes a problem by maintaining a population

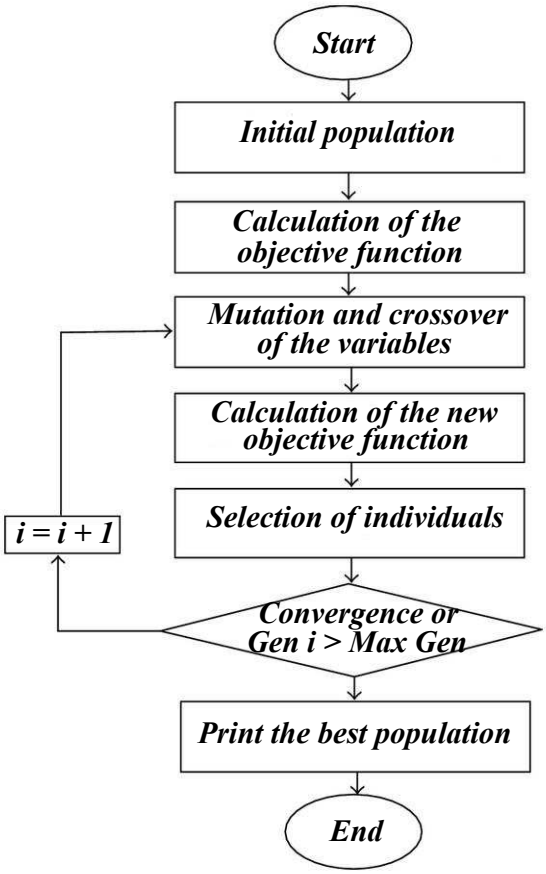


Figure 5.6: DE algorithm.

of candidate solutions and creating new candidate solutions by combining existing ones according to its simple formulae, and then keeping whichever candidate solution has the best score or fitness on the optimization problem at hand. In this way the optimization problem is treated as a black box that merely provides a measure of quality which gives a candidate solution [92] [93].

The differential evolution was developed by Ken Price, in an attempt to solve the Chebychev Polynomial fitting problem. DE is a very simple population based, stochastic function minimizer. The crucial idea behind DE is a scheme for generating trial parameter vectors. The differential evolution algorithm is presented in Fig. 5.6.

The single objective optimization was made with the objective of finding an inductor with a given inductance value, while maximizing the quality factor and minimizing its area; this is achieved through the weighted objective function shown in Eq. 5.2.

$$Objective = 0.7 \cdot min(-Q) + 0.3 \cdot min(Area) \tag{5.2}$$

Several simulations were made in order to obtain inductors with a desired inductance from 1 to 5 nH. It is important to refer that all the optimizations were done with 300 individuals and 300 iterations. The comparison values and curves are shown for each

of the inductors obtained. The physical parameters are given in Table 5.1, as well as the values for inductance and quality factor at 2.4 GHz. All the physical parameters are given in μm, and the inductance in nanohenries.

$L_{Desired}$	n	w	D_{in}	s	L_{model}	L_{EM}	ε %	Q_{model}	Q_{EM}	ε %
1	2	10	123	2.5	1.04	1.01	**2.97**	8.80	9.07	**2.98**
2	3	10	106	2.5	2.10	1.87	**12.30**	11.17	9.85	**13.41**
3	3	10	144	2.5	2.80	2.66	**5.26**	11.32	10.35	**9.37**
4	3	8.03	185	2.5	3.77	3.71	**1.62**	10.24	10.10	**1.39**
5	4	5.63	143	2.5	5.03	4.90	**2.65**	9.21	9.55	**3.56**

Table 5.1: Comparison between the inductance and quality factor value for the optimized inductors.

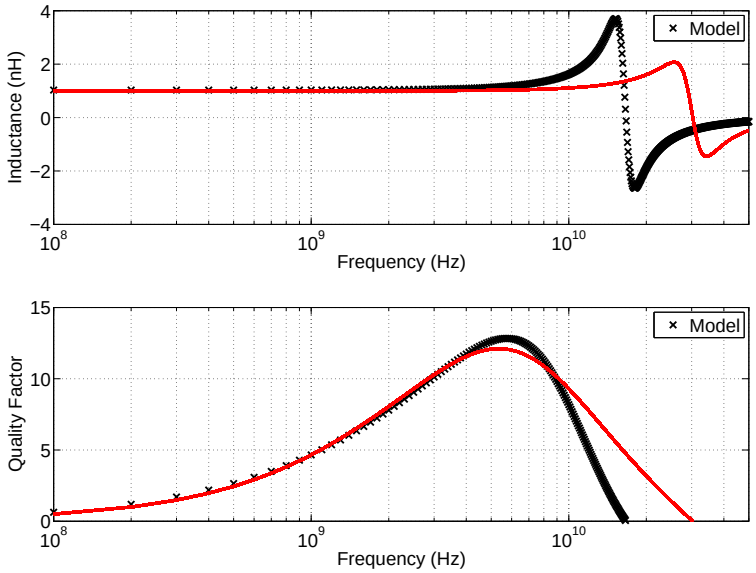


Figure 5.7: EM simulation data (solid line) compared with the model for an optimized 1 nH inductor in a 0-35 μm CMOS technology.

It is possible to conclude that the model can be used in RF design in the design space where the optimization process was developed. The errors observed in the optimization process are usually quite acceptable. It also possible to observe that the inductor that has the highest error has the D_{in} and the w close to its boundaries, which increases the error values. However, the model presents one problem in the optimization process. In some inductors, at the desired frequency, the model is still in the positive slope of the quality factor curve, and in the EM simulation, it is possible to observe that this is no longer true. This means that this inductor should no longer be used at this frequency point. This can be observed for the optimized inductor for 4 nH, in Fig. 5.10 and the inductor shown in Fig. 5.11 is already at the quality factor peak value. This problem may be solved by including some more constraints in order to keep the inductor far from the quality factor

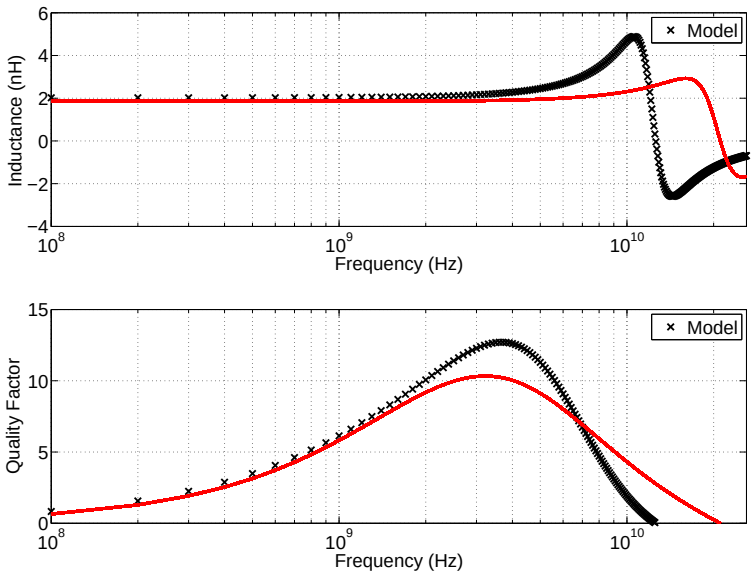


Figure 5.8: EM simulation data (solid line) compared with the model for an optimized 2 nH inductor in a 0-35 μm CMOS technology.

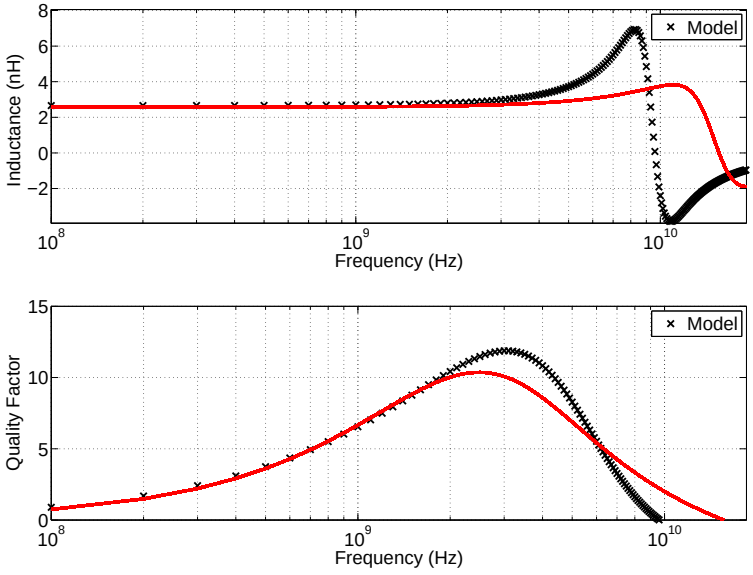


Figure 5.9: EM simulation data (solid line) compared with the model for an optimized 3 nH inductor in a 0-35 μm CMOS technology.

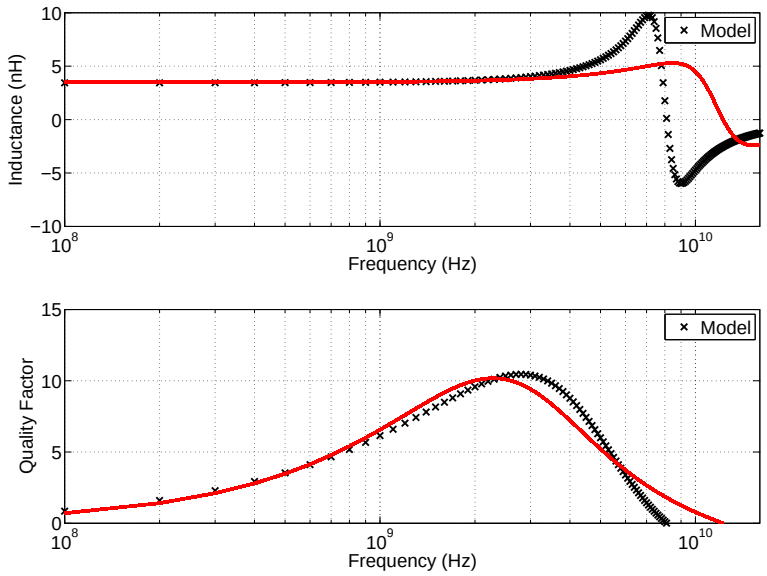


Figure 5.10: EM simulation data (solid line) compared with the model for an optimized 4 nH inductor in a 0-35 μm CMOS technology.

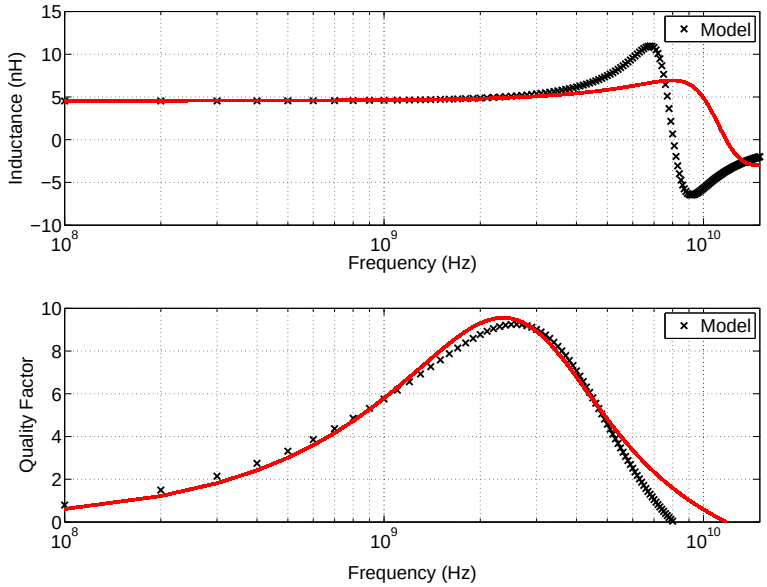


Figure 5.11: EM simulation data (solid line) compared with the model for an optimized 5 nH inductor in a 0-35 μm CMOS technology.

peak value.

As it was explained previously, it was a challenge to use this model at 2.4 GHz, however the model presents an acceptable error value. It is possible to observe that, from DC values up to 1.5 GHz the model presents a perfect fitting.

5.4 Multi Objective Optimization - NSGA-II

Multi-objective optimization is an area of multiple criteria decision making, that is concerned with mathematical optimization problems involving more than one objective function to be optimized simultaneously. For a nontrivial multi-objective optimization problem, there does not exist a single solution that simultaneously optimizes each objective. In that case, the objective functions are said to be conflicting, and there exists a (possibly infinite number of) Pareto optimal solutions [94] [95]. A solution is called nondominated, Pareto optimal, Pareto efficient or noninferior, if none of the objective functions can be improved in value without impairment in some of the other objective values. Without additional preference information, all Pareto optimal solutions can be considered mathematically equally good. Researchers study multi-objective optimization problems from different viewpoints and, thus, there exist different solution philosophies and goals when setting and solving them. The goal may be finding a representative set of Pareto optimal solutions, and/or quantifying the trade-offs in satisfying the different objectives, and/or finding a single solution that satisfies the preferences of a human decision maker (DM).

A multi-objective optimization can be mathematically formulated as:

$$\begin{aligned} &\text{Minimize } F(x); F(x) = \{f_1(x), f_2(x), ..., f_n(x)\} \in \mathbb{R} \\ &\qquad \text{such that: } G(x) \geq 0; G(x) = \{g_1(x), g_2(x), ..., g_n(x)\} \in \mathbb{R} \\ &\qquad\qquad \text{where } x_{Li} \leq x_i \leq X_{Ui}, i \in [1, p] \end{aligned} \tag{5.3}$$

where x is a vector with i design variables, restricting each design variable between a lower (X_{Li}) and the upper (X_{Ui}) limit. The functions $f_j(x)$ with $1 \leq j \leq n$ are the objectives that will be optimized, where n is the total number of objectives. The space that contains all possible solutions is known as feasible search space. The goal of multi-objective optimization is to provide the best trade-offs among the functions $f_j(x)$ in the feasible search space. Obtain the solution to this problem is the objective of the NSGA-II algorithm.

Two different simulations were done with NSGA with 40 individuals and 40 generations, the first one had two objectives: maximizing inductance and maximizing the quality factor, and had three constraints, the inductance curve has to be in the plain bandwidth zone, which means that the inductance value can only vary 10% from the

DC value and the quality factor has to be before the peak value, which means that the quality factor has to be in the positive slope region of the quality factor curve and the area had to be bellow 200 μm. In both simulations one of the constraints was that the quality factor curve had to be rising between 2.4 GHz and 3.1 GHz. In Fig. 5.12 it is possible to observe this simulation in comparison with the same optimization carried out with EM simulations.

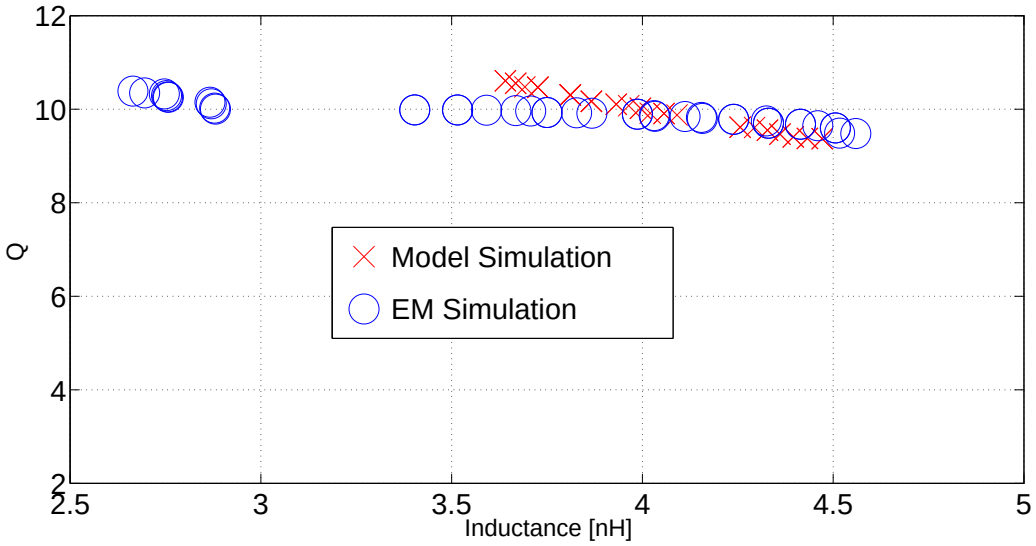


Figure 5.12: Multi-objective optimization with the objective maximizing inductance and quality factor. Comparison between the model and EM simulations for 40 individuals.

It is possible to observe in Fig. 5.12, that the model obtains individuals with higher quality factors at lower inductance values when compared with EM simulation, which means that the model overestimates the quality factor. This fact may be because inductors with lower inductance normally have a higher SRF value, and the capacitance model does not model properly the behaviour of the inductor, therefore inducing higher errors also in the quality factor. All the inductors obtained with the optimization carried out with the model were simulated electromagnetically in order to observe the accuracy of the model. In Table 5.2 it is possible to observe inductors physical parameters and a comparison between the inductance and quality factor values at 2.4 GHz. The average error in the inductance is of 6 % and in quality factor of 3 %, which is quite acceptable as a first stage RF design process. Afterwards this simulation can be used as an insight on the upper and lower limits of the optimization variables to include into an optimization with an EM simulation process. So it may be concluded that the model is trustful for an optimization process. The physical parameters are in μm and the inductance is in nanohenries. It can be seen in Table 5.2, that the inductor with the highest error in inductance and quality factor value, is the one that has the D_{in} equal to 103 μm, which is the smallest D_{in} on the list and is also the closest to the border value on which the model has proven to function. Inductors with D_{in} higher than 125 μm, present small errors, in inductance and quality

n	D_{in}	w	L_{EM}	L_{model}	ε %	Q_{EM}	Q_{model}	ε %
4	129	5,70	4,31	4,47	**3,70**	9,73	9,37	**3,81**
4	103	7,85	3,29	3,64	**9,73**	9,90	10,61	**6,65**
4	123	6,10	4,05	4,26	**4,77**	9,85	9,62	**2,43**
4	118	6,55	3,85	4,09	**5,91**	9,92	9,88	**0,49**
4	116	6,60	3,77	4,02	**6,20**	9,93	9,92	**0,18**
4	109	7,30	3,50	3,81	**8,07**	9,96	10,30	**3,37**
4	106	7,60	3,39	3,73	**8,92**	9,93	10,47	**5,10**
4	115	6,80	3,73	3,99	**6,60**	9,95	10,02	**0,71**
4	111	7,05	3,58	3,87	**7,44**	9,96	10,17	**2,11**
4	126	5,85	4,18	4,36	**4,14**	9,73	9,47	**2,82**
4	105	7,60	3,36	3,69	**9,06**	9,93	10,48	**5,21**
4	127	5,75	4,22	4,40	**3,92**	9,74	9,41	**3,54**
4	104	7,75	3,32	3,67	**9,47**	9,90	10,55	**6,24**
4	125	6,00	4,14	4,33	**4,44**	9,82	9,55	**2,81**
4	117	6,60	3,81	4,06	**6,09**	9,93	9,91	**0,19**
4	113	6,95	3,65	3,93	**7,04**	9,95	10,11	**1,54**
4	128	5,70	4,26	4,43	**3,78**	9,73	9,38	**3,76**
4	124	6,10	4,09	4,29	**4,68**	9,84	9,61	**2,43**
4	114	6,90	3,69	3,96	**6,86**	9,95	10,08	**1,25**

Table 5.2: Inductors physical parameters and comparison between the inductance and quality factor values at 2.4 GHz.

factor. Therefore, it may be stated that the D_{in} is one of the main factors affecting to the model errors. This may be supported by the fact that the model does not include Eddy currents, so when the inductor stops being hollow, the errors increase.

In Fig. 5.13, Fig. 5.14 and Fig. 5.15, it is possible to observe the curves generated with the model and the ones simulated electromagnetically. It is possible to conclude that all inductors comply with the constraints imposed to the optimization and that the curves match.

The inductors generated with the model where simulated electromagnetically and drawn together with the previous simulations in Fig. 5.16. It is possible to observe that the inductors generated with the model (and simulated electromagnetically) give almost the same front-end as that the ones generated with the optimization with the EM simulator. This means that the optimization with the model is reliable and matches quite well the optimization with the EM simulator. With this design flow it is possible to conduct a very fast optimization (with the model), and then simulate only the inductors given by the optimization in a fine tuning operation, to achieve the performance trade-offs quite accurately.

This method will save plenty of time in the design of RF circuits because there is no need to include the EM simulator into the optimization process. So it is possible to use the design flow shown in Fig. 5.17 in order to reduce the simulation time from approximately 50-60 hours (optimization relying on EM simulations) to only 15 hours, with the model

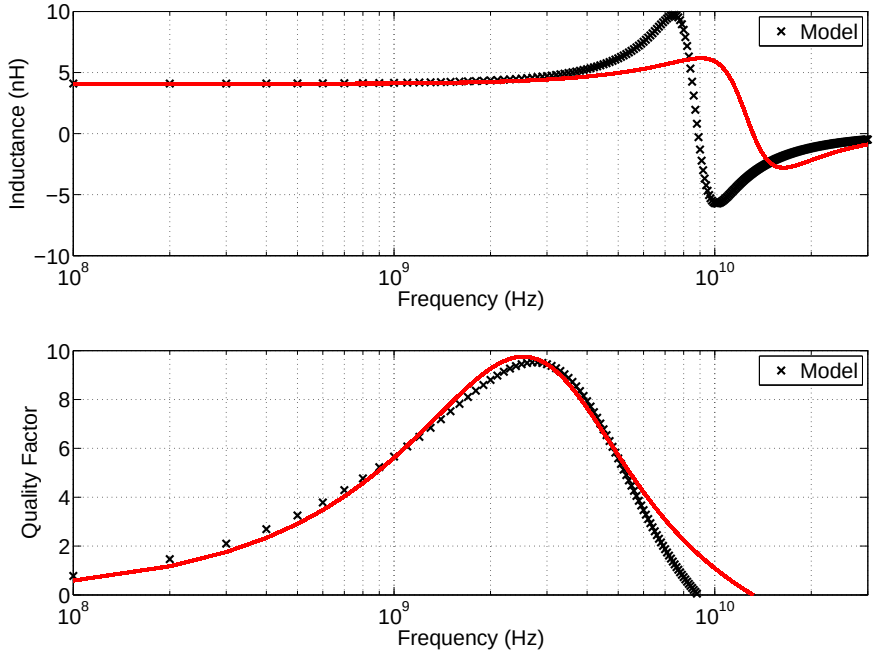


Figure 5.13: First inductor from Table 5.2. Comparison between the model and EM simulation.

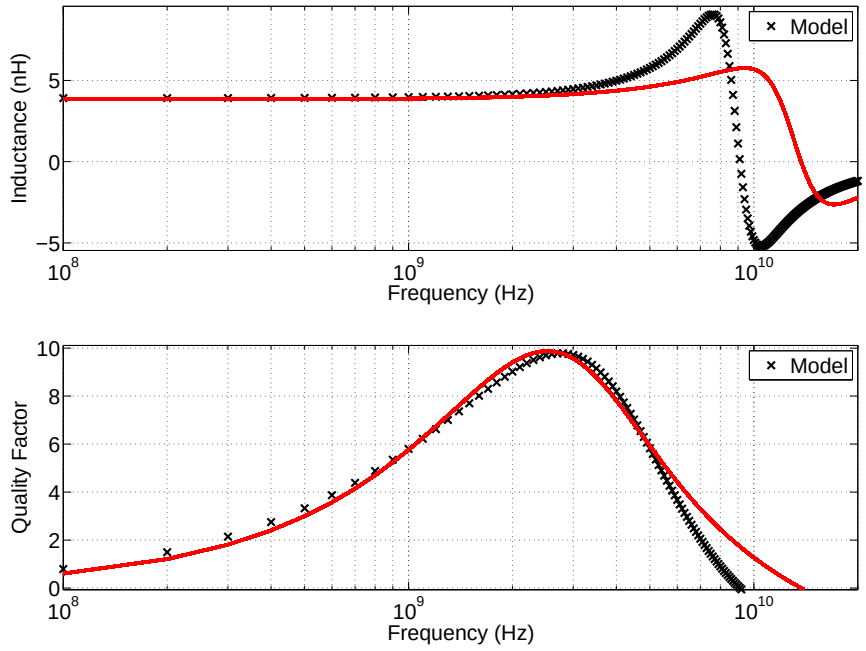


Figure 5.14: Third inductor from Table 5.2. Comparison between the model and EM simulation.

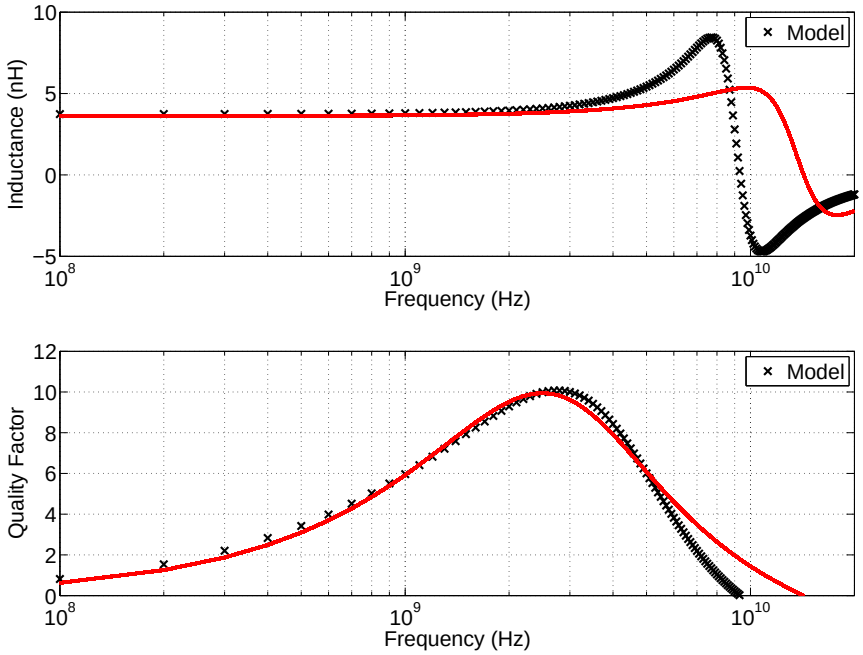


Figure 5.15: Fifteenth inductor from Table 5.2. Comparison between the model and EM simulation.

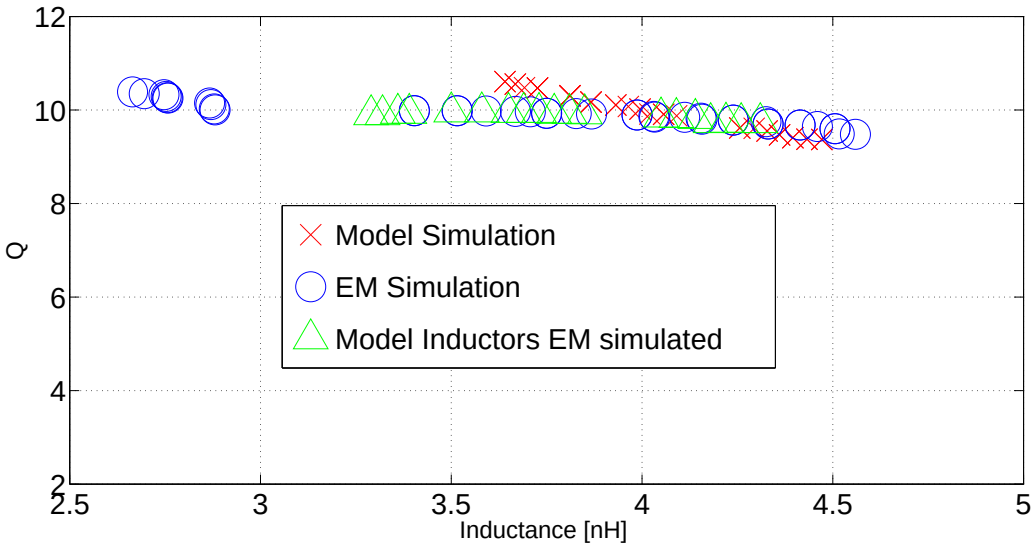


Figure 5.16: Comparison between the optimization carried out with the model, EM simulation and the inductors generated with the model and simulated electromagnetically.

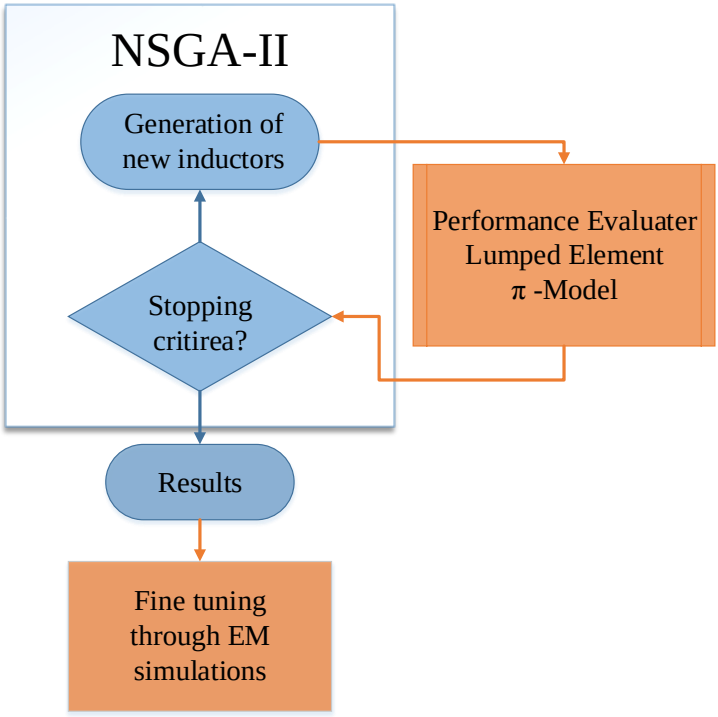


Figure 5.17: Design flow used in order to reduce the design time.

integrated with the optimization tool and afterwards performing a fine tuning operation with EM simulation.

Afterwards, another optimization was carried out. It was important to observe how the model behave itself with the increase of individuals and generations, in order to observe which was the difference between an optimization with 40 individuals and 40 generation and 1000 individuals and 200 generations.

Once the model simulates quite fast (2 minutes for 40 individuals and 40 generations), the time was not an issue on this simulation. In Fig. 5.18 it is possible to observe the same optimization but with a higher number of individuals and generations, with the simulation taking approximately 20 minutes. This way it was possible to observe the maximum pareto solutions that were possible to obtain with this technology.

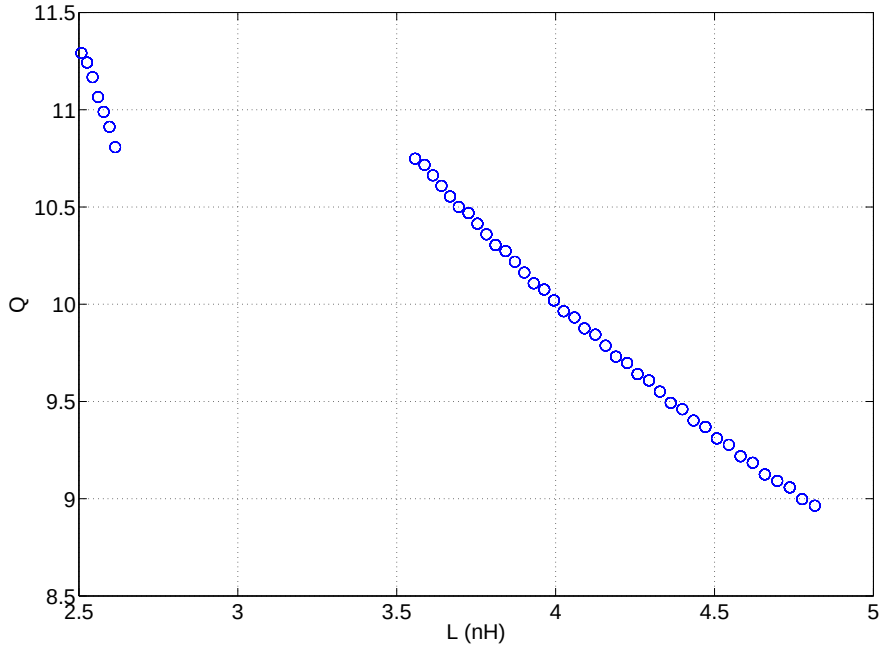


Figure 5.18: Multi-objective optimization with the objective maximizing inductance and quality factor. Model simulation for 1000 individuals.

The second simulation performed had the same constraints but had an extra objective: minimizing the area. The area is an important factor in RF design, due to the high cost of integrated circuits, so it is important to minimize it. This simulation shows the performance trade-off of this technology in respect to the area. In Fig. 5.19 it is possible to observe this simulation in comparison with the same optimization carried out with EM simulation.

It is possible to observe in Fig. 5.19, that the model can approximate the front generated by the EM simulation. This means that the model is suitable to understand the performance trade-offs of the 0.35 μm CMOS technology. It must be said that the model takes up to three minutes to finish the optimization and the optimization with EM simulations can take up to 40 hours, which is also an advantage. So with the model it is possible to make optimizations with 1000 individuals and 200 generations in 20 minutes, something that could last weeks in EM simulations. The result of the model simulations is given in Fig. 5.20.

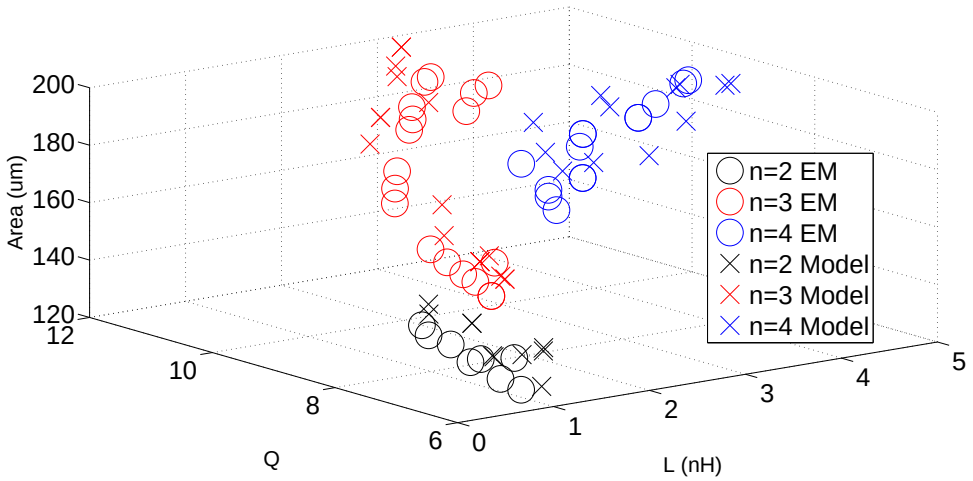


Figure 5.19: Multi-objective optimization with the objective of minimizing the area and maximizing inductance and quality factor. Comparison between the model and EM simulations for 40 individuals.

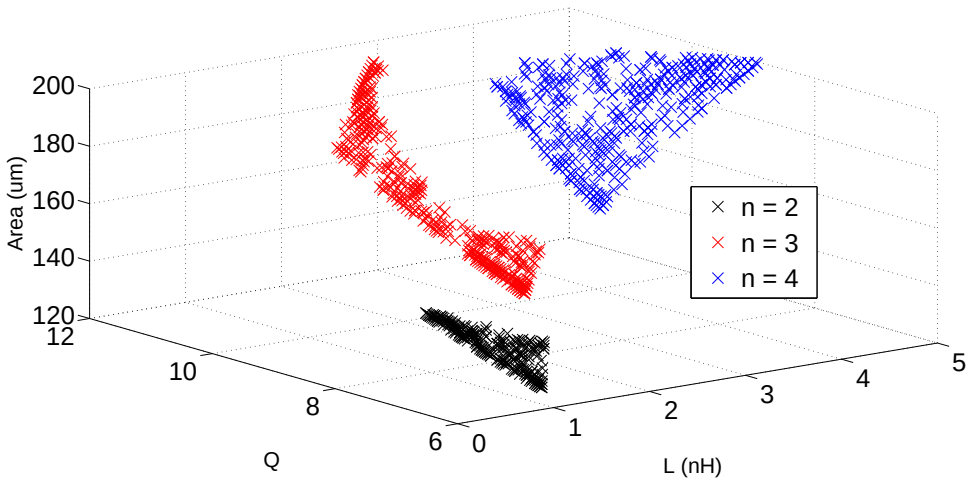


Figure 5.20: Multi-objective optimization with the objective of minimizing the area and maximizing inductance and quality factor. Model simulation for 1000 individuals.

6

Conclusion and Future Work

In this work an efficient lumped-element model to characterize integrated inductors is presented. The model uses analytical expressions to define the lumped elements where fitting factors are included to obtain better accuracy. The model is able to predict the inductance and the quality factor values with relative accuracy for different physical topologies and technologies. These results have been proven against the field solver ASITIC and EM simulations for equal width and tapered inductors. A statistical study for a large number of different inductors was also performed. These comparisons and studies served to determine the ranges of physical parameters in which the model can be used in the design of RF circuits. The model was also integrated in two different optimization processes and the results validated against EM simulation.

As future work, the model can be fitted to smaller frequency ranges in order to obtain higher accuracy. The complexity of the model can also be increased, adding elements to the equivalent circuit. When integrated into an single-objective optimization process different weight function can be used in order to observe how the model reacts to these changes. Several techniques can be explored and compared. For example, in an optimization process, a simulation can be done using only the analytical model, using the analytical model in the first stages of the optimization and then EM simulations in the final optimization. These would result in a faster simulation while keeping the accuracy of the simulation. The model can also integrate different fitting factors for different frequency values. The last possibilities can also be extended to multi-objective optimization. Afterwards, the model can be used to design RF circuits, where inductors will be needed.

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